Introduction

Overview

The Catalyst test system contains a variety of advanced instrumentation integrated into a versatile test system configured to customer device testing needs.

These instruments include:

- DC sources and meters
- AC sources, meters, and digitizers
- Time measurement instruments
- High speed digital channels

Some of these instruments include OEM products as components. OEM products are an integral part of the instrumentation; their calibration requirements are integrated into the calibration strategy defined in this manual.

Note

The calibration requirements for an OEM product integrated into a Catalyst test system may vary from the requirements defined in the OEM manuals.

In all cases, the Teradyne calibration procedure supersedes the OEM procedure. In the cases where an OEM procedure can be alternatively used, such as the PMM, the alternative calibration procedure is described in the External/Internal Calibration and Traceability Procedures section of this manual.

How to Use This Manual

To gain an understanding of the Catalyst calibration process, the first-time reader should do the following:

- Read section Introduction to understand calibration and traceability processes of Catalyst systems.
- Review the definitions in Appendix B. Terms in this manual may differ from those used in your company. Please review the definitions to avoid confusion.
- Read the specification support summary section for relevant instruments. This provides the following information for each instrument:
  - Calibration schedule
  - Calibration equipment
  - Description of the instrument calibration path for key instrument specifications
  - Description of the instrument traceability path for key instrument specifications

Calibration Process Overview

Internal System Calibration Path

To fully understand multilevel calibration it is important to first understand the test system architecture. There are three categories of instrumentation, as shown in figure Internal Calibration Path.

- Internal system references
- Internal transfer standards
- Test system instrumentation

Internal System References

These internal references are not directly accessible to the user as system instrumentation. Rather, they serve as the lowest level of internal reference. They may be used to generate a master signal during system usage (LA703 10 MHz reference) or for self-test and autocalibration purposes (AD412 DC reference). These references have defined drift, resulting in the need for periodic adjustment. Some of these references are base system references used by multiple instruments while others are references dedicated to a specific instrument type. Dedicated tests are present only when the corresponding instrument is present in the system.

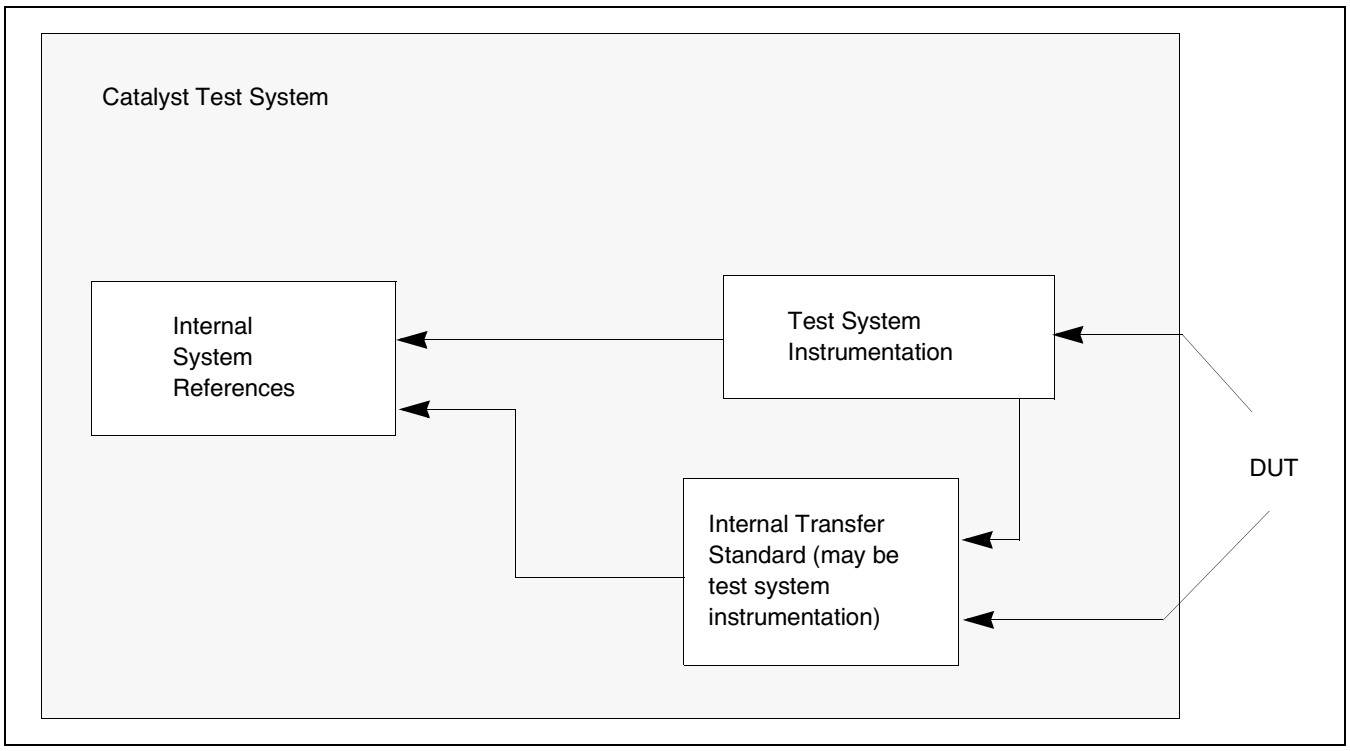
Internal Transfer Standards

These instruments transfer the accuracy of fundamental system references to other instruments. This action is often not directly observable, as in the use of the standard voltage current (V/I) source used in the calibration of analog pin units (APUs). These internal transfer standards may also be accessible to the user as test system instrumentation.

Test System Instrumentation

These instruments are directly accessible test system instrumentation. The accuracy of many of the source or measurement functions of the instruments is linked directly or through an internal transfer standard to internal system references via internal software calibration processes.

Some of the source or measurement functions of these instruments do not have accuracy linked to any other system reference (the instrument carries its own “standard”). An example would be an instrument whose output levels are fixed by component values whose drift is expected to remain within design tolerances for the life of the instrument. Traceability of these instruments is established by direct comparison with external standards as part of the level 4 field calibration process.



Internal Calibration Path

The simplified view of the calibration path, as shown in figure Internal Calibration Path, shows that the internal calibration flow can be different for different instruments. Different specifications within the same instrument can follow a different calibration path.

External System Calibration Path

The calibration path extends outside the system via two types of external calibration, each using instrumentation defined by Teradyne. These calibration paths are shown in figure Internal Calibration Path with First Level External Link.

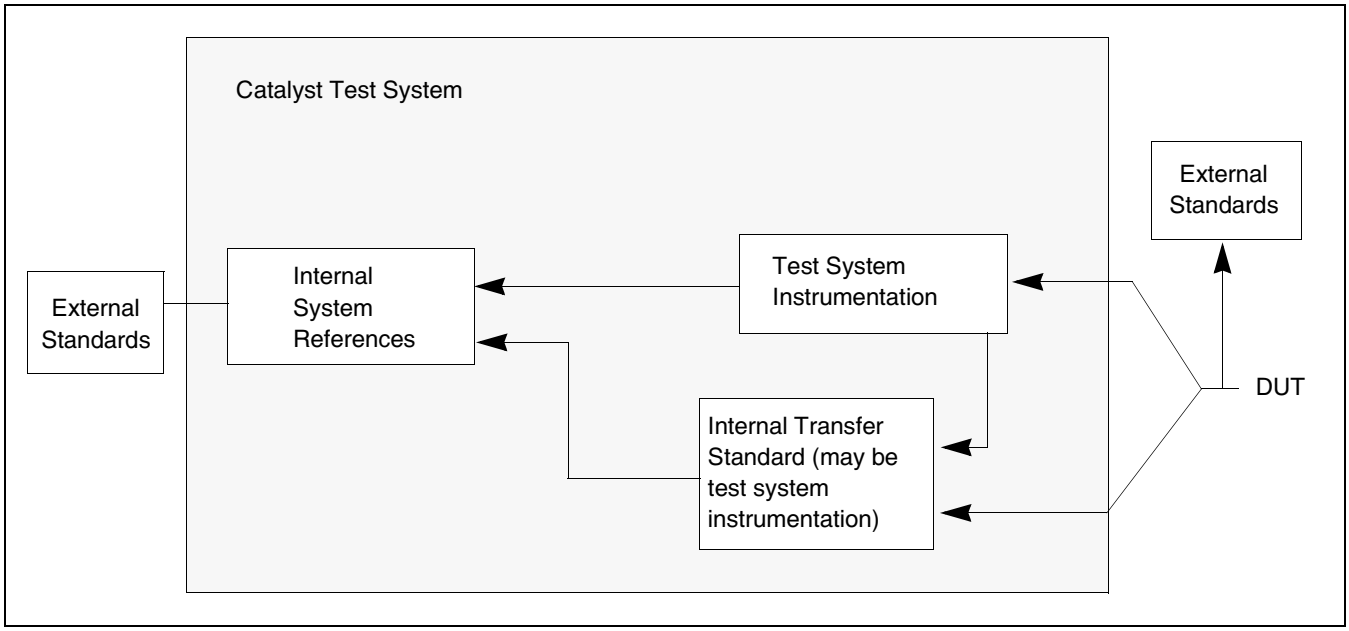
Calibration of Internal References

External instruments are used to calibrate (measure and adjust) the internal system references.

Calibration for Traceability of Test System Instrumentation

External instruments are used to calibrate traceable (measurement comparison only) test system instrumentation specifications at the user interface.

Some instruments have inherent accuracy not maintained by periodic comparison to internal system references (for example, AC instrument amplitude accuracy). To maintain traceability of these quantities a direct comparison with external standards is required. This is the basis for requiring the second type of calibration (measurement comparison only) for traceability.



Internal Calibration Path with First Level External Link

Calibration Levels

To gain an understanding of the calibration process options, it is important to identify the four levels of calibration. The table Calibration Levels defines which levels are required to maintain system specification performance and how system specification traceability is established:

Calibration Levels

Level	Calibration Type	Purpose	Traceability	Performance
Level I	Internal autocalibration	Adjust system instrumentation via internal standards.	via Level III	Required
Level II	Internal and external system checkers	Verify system performance and functionality. Provide full verification against specifications as permitted by internal paths.	via Level III	Required
Level III	External calibration of internal system references	Measure and adjust internal system references using traceable external equipment.	via external instrumentation	Required
Level IV	Optional device interface performance traceability	Provide additional traceability via a direct path from the system instrumentation device interface to an external reference standard.	via external instrumentation	Optional

The higher the level, the more comprehensive the calibration, provided that all lower levels are also maintained.

Teradyne recommends that levels 1, 2, and 3 be implemented to maintain system specification performance. For customers whose process controls require documented evidence of instrumentation performance at the device interface, level 4 provides a traceable path.

Note

To achieve traceability, all external equipment must be traceable to national or international standards via a user-provided traceable path.

However, Teradyne understands that different sites may need or want to develop a modified calibration strategy that best fits their company needs.

To further aid customers in tailoring a calibration strategy that best fits their equipment needs, several calibration products and services are provided. These are identified and defined in the section Calibration Products and Services.

Level 1: Internal Autocalibration

These programs are executed at job run time to measure and electronically adjust the test system instrumentation. The programs use internal system references to maintain the published accuracy specifications.

Level 2: Internal/External System Checkers

These programs are executed at the recommended interval to verify proper operation of the functions of a specific instrument or subsystem. In some instances where the accuracy of the internal calibration path permits, these checkers provide full calibration against specifications. Most often they are self-test (ST) programs that do not require the use of any external fixtures or instrumentation.

A small number are maintenance and installation (mi) programs requiring the use of some type of external fixtures or instrumentation. These programs are typically used to check the final connection path out of the system.

Level 3: External Calibration of Internal System References

These programs are executed at some regularly defined interval. They use external standards to measure and adjust internal system references. Since these references have defined drift parameters, these programs are designed to adjust these references. Some of these references are base system references used by multiple instruments while others are references dedicated to a specific instrument type. Traceability of the internal system references can be maintained using these programs provided that traceable external equipment is used and proper procedures are followed.

Level 4: Optional Test System Instrument Traceability Processes

These programs are executed at some regularly defined interval to measure test system instrumentation performance to the user interface. This performance is traceable to national or international standards. These programs do not perform any adjustment of system instruments or references and are not required to maintain system performance. They are used to establish and maintain system instrument traceability.

Calibration Products and Services

Calibration Products

System Calibration Certificate

This is provided with every system purchased. It is a signed certificate of calibration that certifies the system has been fully calibrated by Teradyne prior to shipment.

Autocalibration (Level 1)

This is provided with every system purchased. It automatically calibrates the test system instrumentation.

- Software: Provided with system.
- External Fixtures: None required.
- External Equipment: None required.
- Execution Procedures: See section External/Internal Calibration and Traceability Procedures.

System Checkers (Level 2)

These are provided with every system purchased. They verify proper operation of the functions of the instrumentation.

- Software: Provided with system.
- External Fixtures: Purchased separately (required for mi checkers only).
- External Equipment: None required.
- Execution Procedures: See section External/Internal Calibration and Traceability Procedures.

System Reference Calibration Processes (Level 3)

These are provided with every system purchased. These give the customer the capability to calibrate (including adjustment) all internal system references.

- Software: Provided with system.
- External Fixtures: Purchased separately.
- External Equipment: Provided by customer.
- Execution Procedures: See section External/Internal Calibration and Traceability Procedures.

Optional Traceability Processes (Level 4)

You can choose to purchase GFS Traceability Process Support (Level 4) (see section Calibration Services) or to perform the traceability process yourself. To do the process yourself, you need the following items to generate traceable performance data at the device interface. These are not provided with the system.

- Software: Purchased separately.
- External Fixtures: Purchased separately.
- External Equipment: Provided by customer.
- Execution Procedures: Included in section Traceability of Test System Instruments (Level IV Calibration) of this manual.

Calibration Services

GFS Maintenance Support (Level 2)

This Teradyne service enables GFS maintenance engineers to execute preventive maintenance and/or system failure analysis and repair support.

GFS Internal Reference Calibration Support (Level 3)

This Teradyne service enables GFS service engineers to perform the internal system reference calibration processes.

GFS Traceability Process Support (Level 4)

Under this service, the customer contracts with Teradyne to perform the field traceability processes. Teradyne provides the software, special fixtures, all external equipment (using rentals), and the labor to execute the field traceability processes.

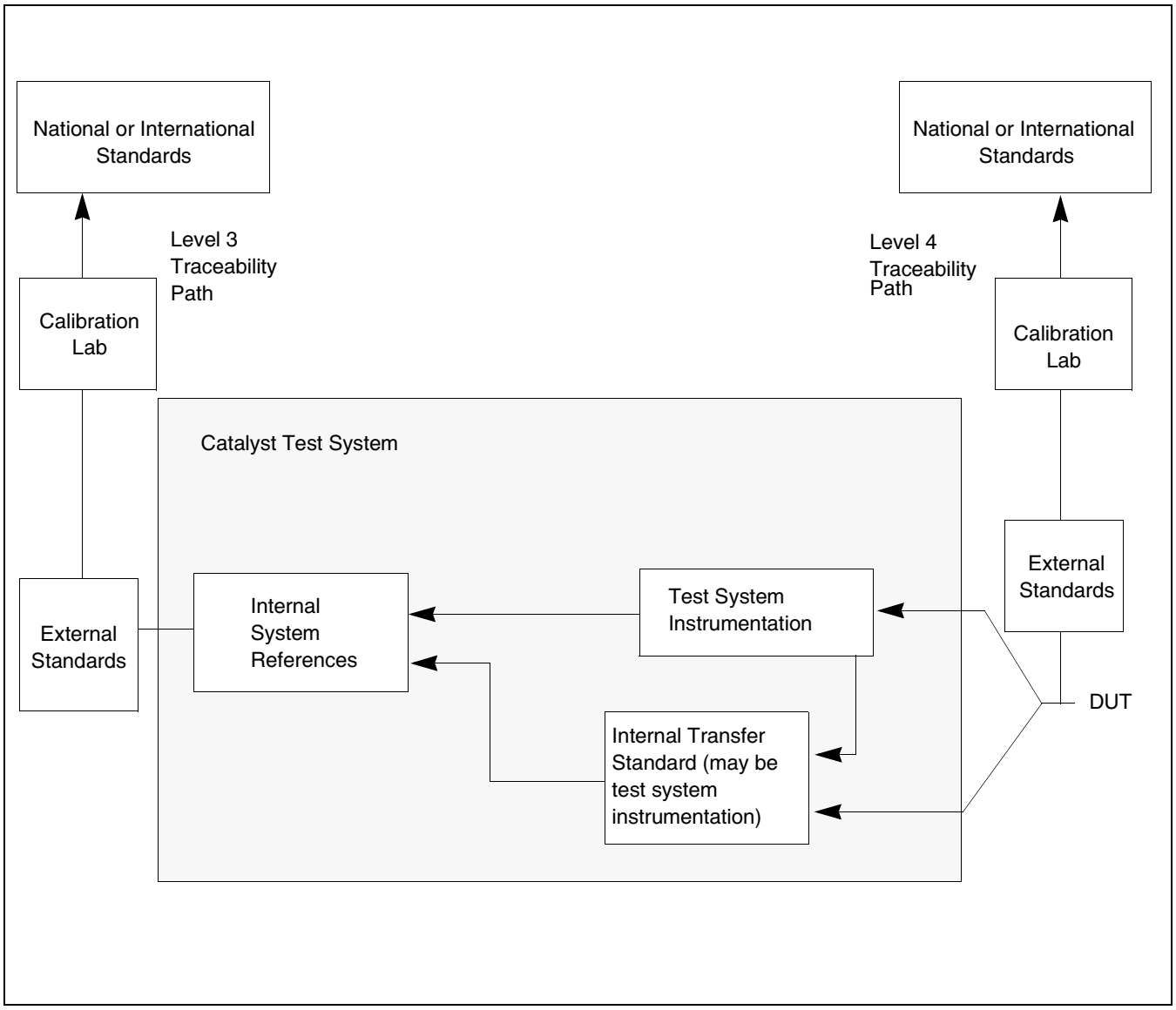
Specifications

To verify any test systems accuracy specifications in this document, read the Catalyst System Specifications manual (pn 553-403-56). This is a controlled document and contains all test system accuracy specifications.

Traceability

The figure Traceability Flow Block Diagram details the calibration and traceability path for device measurements made on Catalyst instrumentation. Traceability of the Catalyst test system instrumentation is achieved by following the processes outlined in this manual and using external standards calibrated and traceable through a qualified calibration lab to a national standard.

It is the user's responsibility to define and support the traceability path. If the user contracts with Teradyne to provide the field calibration service, the traceability path is through the equipment rental service. Availability of appropriately traceable test equipment on site is the responsibility of the user unless other arrangements are made with the local Teradyne service office.



Traceability Flow Block Diagram

Replacement of System Reference

It may be necessary to replace a system reference. If the new reference is precalibrated, then only level 1 and 2 processes need to be executed after replacing the reference. If the new reference is not precalibrated, then levels 1, 2, and the appropriate level 3 process must be executed with the new reference.

Overview

This chapter includes the following three matrixes:

- Calibration Process Schedule Matrix
- Calibration Equipment Matrix
- Estimated Time Matrix

Calibration Process Schedule Matrix

The table Catalyst Field Calibration Process Summary is a matrix of the processes described in this manual. The scheduled intervals of these processes varies from every 4 hours to once a year. All the processes listed in the matrix can be performed by properly trained customer personnel. There are also service support packages offered by Teradyne that include total coverage by Teradyne personnel.

For more information regarding specified autocalibration intervals, refer to the IMAGE Base Language Manual (pn 553-403-17). Procedures should be run in the order listed due to some procedure dependencies. See table Catalyst Field Calibration Process Summary for further process dependency information.

Calibration Equipment Matrix

The lists all the required equipment for quarterly or annual processes. Each row identifies the required type of instrumentation. For the Teradyne tool kits necessary for calibration, see the table Teradyne Tool Kits. For the addresses of the manufacturers of this equipment see section Non-Teradyne Equipment Information.

Estimated Time Matrix

The estimated time matrix contains the estimated execution times for each process.

Catalyst Field Calibration Process Summary

	Required			Optional
Calibration Interval	Level 1 Internal Autocalibration	Level 2 Internal/External System Checkers	Level 3 External Calibration of Internal References	Level 4 Additional Traceability Process for System Instruments
Specified Autocalibration Interval	Internal Automatic Calibration (Level 1)			
Weekly	Internal Automatic Calibration (Level 1) Autocal is performed with System Check.	System Check -brief (brief mode) System Check Continuity Checks -weekly: -catalyst_continuity_mi (default) Precision Multimeter (PMM)		
Monthly	Internal Automatic Calibration (Level 1) Autocal is performed with System Check.	System Check- full (full mode) System Check Continuity Checks -monthly: -catalyst_continuity_mi (default) Precision Multimeter (PMM)3		
Quarterly	Internal Automatic Calibration (Level 1) Autocal is performed with System Check.	System Check - full (full mode) System Check Continuity Checks -Monthly: -catalyst_continuity_mi (all tests) Precision Multimeter (PMM)	- dcrefcal Equipment and Setup for dcrefcal - hcurefcal Equipment and Setup for dcrefcal - pmm_xcal_mi pmm_xcal_mi Procedure	
Annually	Internal Automatic Calibration (Level 1) Autocal is performed with System Check and Traceability Programs (CV).	System Check - full (full mode) System Check Continuity Checks -monthly: -catalyst_continuity_mi (all tests) Precision Multimeter (PMM)	Base System: - dcrefcal Equipment and Setup for dcrefcal - freq_ref_mi LA703 10 MHz Master Reference Module Calibration Setup - hcurefcal Equipment and Setup for dcrefcal - pmm_xcal_mi pmm_xcal_mi Procedure	-hsd_edge_cv hsd_edge_cv -atms_cat_cv atms_cat_cv -plf_cat_cv cat_plf_cv -lfac_cat_cv cat_lfac_cv -vhfd_catalyst_cv VHF Digitizer CV -vhfawg400_diff_catalyst_cv vhfawg400 diff cv -vhfawg1200_catalyst_cv vhfawg 1200 cv vhf -tjd_cv tjd_cv -uw6000_cv Calibration Procedure

Calibration Equipment Detail Matrix

Manufacturer	Model	Description	Options	GPIB[a]	Where-Used	
					Quarterly	Annually
Agilent	HP 3458A	Digital Multimeter w/High Stability Option	option 002	10	DC, HCU	DC, LFAC, PLF, HCU
Datron	4910	Reference Standard		N/A	PMM b	PMM
Fluke	742A-10k 5440A-7002	Reference Standard Low Thermal EMF Cables		N/A	PMM	PMM
Hewlett-Packard	HP53131A	Frequency Counter	option -010 3 week calibration c	11		freq_ref_mi
Hewlett-Packard	HP8902A	Measuring Receiver		14		VHFAWG, VHFD, VHFCW
Hewlett-Packard	HP11722A	100 KHz - 2.6 GHz Sensor Module		N/A		VHFAWG, VHFD, VHFCW
Hewlett-Packard	HP8657A	Synthesized Signal Generator		7		VHFD
Hewlett-Packard	HP54750	Digitizing Scope		7		HSD
Hewlett-Packard	HP54751A	2 Channel 20 GHz Plug-in		N/A		HSD
Hewlett-Packard	HP8657 (A or B)	Signal Source		7		TJD
Hewlett-Packard	HP E4418 (A or B)	Power Meter	GPIB			UW6000 SRC
Hewlett-Packard	HPE4412A	Power Sensor				UW6000 SRC

a. GPIB communications are used for most Level III and Level IV processes. It is necessary to configure the measurement device with the appropriate address prior to starting the test. Note: In the case of the HP8902A unit, the address selection switches are embedded within the unit and must be set by qualified individuals.

b. The PMM instrument specification is time dependent. Teradyne provides specification detail at quarterly and annual intervals. Consult the PMM ESSD to determine instrument performance accuracy and match the appropriate calibration period with the test accuracy requirements.

c. The internal time base of the HP53131A must have been calibrated within the three weeks prior to conduct of the freq_ref_mi process in order to enssure the desired accuracy (±0.2 Hz @ 10 MHz).

Estimated Time Matrix (Level 1)

Program	Estimated Time
calibrate -dc	1 minute
calibrate -apu	20 sec + 3.5 sec/pin
calibrate -pmm	2.2 min. dcv/1.1 min. acv /11 min. ohms
calibrate -tms	1.25 minutes
calibrate -plfdig	30 seconds/instrument
calibrate -plfsrc	10 seconds/instrument
calibrate -vhfawg	5 seconds/instrument
calibrate -vhfcw	15 seconds/instrument
calibrate -vhfd	15 seconds/instrument
calibrate -hsd	3 minutes/cal_set (256 channels)
calibrate -tjd	5 seconds/instrument

Estimated Time Matrix (Level 2)

Program	Estimated Time
system check -brief	2.5 hours
system check -full	3.5 hours (256 channels)
catalyst_continuity_mi	5 minutes

Estimated \Time Matrix (Level 3)

Program	Estimated Time
dcrefcal	20 minutes
freq_ref_mi	20 minutes
hcurefcal	20 minutes
pmm_xcal_mi	30 minutes

Estimated \Time Matrix (Level 4)

Program	Estimated Time
hsd_edge_cv	12 seconds/channel
plf_cv	37 minutes/instrument
vhfawg_xxx_cv	25 minutes/instrument
vhfcw_cv	25 minutes/instrument
vhfd_cv	30 minutes/instrument
atms_cv	10 minutes
lfac_cv	35 minutes/instrument
tjd_cv	15 minutes
uw6000_cv	5 minutes

Teradyne Tool Kits

Teradyne Part Number	Description	Options	Where-Used	
			Quarterly	Annually
806-166-05	Kit, Catalyst Continuity		Continuity	Continuity
803-800-00	Kit, Level III Calibration	Specify kit # 803-800-02 instead if performing pmm_xcal_mi	All	All
803-804-00	Kit, Multipurpose DIB		PMM	PMM, HSD, All VHF, ATMS, TJD
803-806-00	Kit, Level IV Base			All Level IV
803-808-00	Kit, PLF/LFAC CV			PLF, LFAC

PMM instrument performance is time dependent. Customer performance requirements dictate the appropriate calibration intervals. Regardless of the selected interval, the specified equipment and fixturing is only required if the PMM is calibrated in the test system. See Alternate DC Calibration for an alternate calibration method.

Non-Teradyne Equipment Information

Non-Teradyne equipment required for the traceability processes may be obtained from the following manufacturers:

- Hewlett-Packard Company
  US Telephone: 1-800-333-1917
  Outside US: 208-344-4809
- Fluke Corporation
  P.O. Box 9090
  Everett, WA 98206
  US Telephone: 1-800-443-5853
  Outside US: 206-356-5500
- Todd Systems Inc.
  50 Ash St.
  Yonkers, NY 10701
  US Telephone 914-963-3400
- Datron Instruments Inc.
  3401 SW 42nd St.
  Stuart, FL 33494
  US Telephone 305-283-0935

Overview

This chapter provides detailed instructions for calibration of the Catalyst test system. The chapter is divided into three sections:

- Internal Automatic Calibration - Occurs automatically at test program load time.
- Internal and External System Checkers - Invoked from the Checkers menu.
- External Calibration Procedures for Internal References - Performed at system output jacks by Maintenance Engineers using specified electronic test equipment.

Internal Automatic Calibration (Level 1)

Note

The system under calibration, the environment, and any external instruments must be stable with respect to temperature and humidity to ensure accuracy of these procedures.

Automatic calibration uses the internal system DC and frequency references to calibrate many of the test system instruments. Automatic calibration for most instruments is invoked automatically at test program load time. To activate the automatic calibration feature when loading a test program, include `-autocal` on the load command line.

As with other load command options, this switch can also appear in a `.load` file. After a test program is loaded, automatic calibration can be activated by using the `calibrate` command. The command accepts the switches `-autocal` and `-noautocal` on the command line. When automatic calibration is on, the test system automatically calibrates any of the instruments whose current calibration is invalid.

Instruments Calibrated During Autocalibration

- DC subsystem

- Advanced time measurement subsystem (ATMS). ATMS is a full calibration including path length correction. It is performed once for every test head in the test system. This takes place only if the ATMS is used in the test program.
- Analog pin units (APUs). Calibration takes place only if APUs are used in the test program.
- High-speed digital subsystem (HSD), if necessary. HSD calibration takes place when a `start hsd_cal_set` statement is encountered in the test program.
- Precision low frequency source and digitizer (PLF). Calibration takes place only if the PLFSRC and PLFDIG are in the system and one or both are used in the test program.
- Very high frequency continuous wave source (VHFCW). Calibration takes place only if the VHFCW source is used in the test program.
- Very high frequency arbitrary waveform generator (VHFAWG). This Calibration takes place only if one of the VHFAWG instruments is used in the test program.
- Very high frequency digitizer (VHFD). Calibration takes place only if one of the VHFD instruments is used in the test program.
- High speed sampler (HSS). Calibration takes place only if the HSS is used in the test program.
- Time jitter digitizer (TJD). Calibration takes place only if the time jitter digitizer is used in the test program.
- Precision multimeter (PMM). Calibration takes place only if the PMM is used in the test program.

The need for calibration is checked before each run of the test program. This happens either when the `run` command is issued or when a start signal arrives from an enabled handler or prober.

Each instrument requiring internal calibration (level 1) can become invalid for a number of reasons. For example:

- Time elapsing (usually 4 hours, but can be different for some instruments).
- Temperature change greater than specified limits (checked only for some instruments such as the HSD).
- Power source drift (checked only for some instruments, such as the HSD).
- System power cycle (checked only for some instruments, such as the DC subsystem).
- Execution of the `initialize` command.

Validity

If an instrument calibration is invalid, the instrument cannot be used to make measurements. If an instrument with invalid calibration is used, the IMAGE software issues a run-time error. Run-time errors can be ignored (using `set error ignore`); however, measurements made are not valid.

Using autocal is the recommended method to keep a system calibrated during production testing. This method is described in the following topic.

Autocalibration

Autocalibration can be turned on only by using the `-autocal` switch on the load command line, or in a load file statement. Autocalibration is not on by default nor can it be forced to invoke by default. This is due to the number of test programs written before autocalibration was introduced. Potential incompatibility with the functionality of autocalibration can result. Autocalibration is turned off by using the `calibrate -noautocal` command.

When autocalibration is turned on, the state of every instrument used in the test program is checked before each test program is executed. If an instrument's calibration has expired, the instrument is calibrated before the test program runs.

Note

When multiple same-type instruments are present in the test system, calibration must be performed for all those instruments individually.

Loading a test program does not automatically force calibration. When `run` is typed, the tester determines that calibration is required. The DC subsystem and ATMS are calibrated before running the test program. The program is then started. When a start `hsd_cal_set` statement is encountered, the HSD subsystem is calibrated. The program then runs normally.

IMAGE does not take into account programs that call calibration themselves. If the `-autocal` switch is used with a program that issues a tl_system `calibrate -DC` command, for example, the DC subsystem is calibrated twice.

Use of `cron` with calibration commands is not recommended.

Many of the instrument calibration routines use the DC subsystem as part of their calibration process. If you do not use the `-autocal` function and choose to individually calibrate instruments using the `calibrate` command, then always calibrate the DC subsystem before calibrating any other instruments.

For special circumstances, you can set the calibration interval from a test program by using one of the following functions:

```
extern void tl_hsd_set_cal_interval();
extern void tl_tms_cal_set_interval();
extern void tl_apu_cal_set_interval();
extern void tl_plfs_cal_interval();
extern void tl_plfd_cal_interval();
extern void tl_vhfcw_cal_interval();
extern void tl_uhfsrc_cal_interval();
extern void tl_vhfawg_cal_interval();
```

These functions take one parameter: the number of seconds of the calibration interval. To set the interval for DC subsystem calibration to 5 hours instead of 4 hours, use

```
extern void tl_dc_cal_set_interval();
     tl_dc_cal_set_interval(60*60*5);
```

The exception is `tl_hsd_set_cal_interval()` which takes two parameters:

```
void tl_hsd_set_cal_interval(which, secs)
int which; /* 0 => set interval to recalibrate
(default 1 year) */
/* 1 => set interval to check environment
(default 20 mins) */
int secs; /* desired interval in seconds */
```

These functions are *not* required for normal use. Use them only in special circumstances.

Consult the following user manuals for more information on internal system calibration (level 1):

- IMAGE Base Language Manual - Calibration (pn 553-403-17).
- Catalyst Instrumentation Manual - HSD Calibration (pn 553-403-58).

Also refer to individual instrument sections for instrument-specific calibration information.

DC Subsystem

Calibrate the DC subsystem, including all present sources, voltmeter, and DUT sources, using the command

```
calibrate [-station #] -dc [-file | -verbose]
```

This command also calibrates any HCUs in the test system.

As calibration proceeds, the checkers windows display status messages, including:

- Source currently being calibrated
- AD412 reference card serial number

- Date of last calibration
- Result of calibration (passed, failed, or aborted)

Calibration Messages

Messages are shown in the current station window or in the station window specified using the `-station #` option. An example of calibration output is:

```
calibrate -dc

Starting calibration of the DC sources
Data Retention Verified
Reference serial number 851721
Last reference calibration on Sept. 12, 1989
Calibrating Voltmeter
Calibrating Source 1
Calibrating Source 2
Calibrating Source 3
Calibrating Source 4
Calibrating Source 5
Calibrating Dut Source 1
Calibrating Dut Source 2
Calibrating Dut Source 3
Calibrating Dut Source 4
Calibration complete
DC source calibration complete
```

The `-file` option sends a detailed summary of the calibration to a date and time-stamped log file in the following directory:

```
/image/tester/<hostname of tester computer>
/dccal_log_<DATE:HR:MN>
```

The `-verbose` option sends this detailed summary to the station window.

Calibration in the Debug Display

The calibration status, including the date and time of the last calibration, is shown in the DC debug display. If a source failed the last calibration, a double asterisk (`**`) appears after the information line for that source.

Calibration Functions

IMAGE includes several functions related to DC subsystem calibration. One of these, `tl_dccal_subr(0)`, allows you to initiate calibration from a test program. Additional functions are as follows:

`tl_dc_cal_set_interval()`
Sets the autocalibration interval.

`tl_dccal_status(inst)`
Returns the calibration status of each DC subsystem instrument.

`tl_dccal_time()`
Reads the time since the last calibration and the calibration status.

Analog Pin Units (APU)

Calibrate analog pin units (APUs) using the command

```
calibrate -apu
```

This command calibrates all APUs in the test system. As the calibration routine executes, the following messages are displayed:

```
Starting calibration of the APU
Analog Pin Unit Calibration
```

```
Starting Voltage Force Calibration
Starting Voltage Measurement Calibration
Starting Current Force and Measurement Calibration
Starting APU Native Voltage Measurement Calibration
Starting APU Native Current Measurement Calibration
APU Calibration Complete
```

You can also calibrate APUs from a test program by using the statement

```
start apu cal;
```

The following function returns the number of minutes since the last APU calibration:

```
int tl_apucal_time()
```

Precision Multimeter (PMM)

To make sure that the precision multimeter (PMM) meets its rated accuracy specifications, it must be calibrated. Calibrate the PMM using

```
calibrate [-station #] -pmm -dcv -acv -ohms
```

where

`-station #` Perform calibration in the specified station window

`-pmm` Perform calibration of all the PMM modes. This calibration takes 12 minutes.

`-dcv` Perform calibration on the DC voltage modes of the PMM. This calibration takes 2.2 minutes.

`-acv` Perform calibration on the AC voltage modes of the PMM. This calibration takes 1.1 minutes.

`-ohms` Perform calibration on the resistance modes of the PMM. This calibration takes 11 minutes.

You can specify one calibration routine or several.

Note

Do not interrupt calibration by using Ctrl-C. Interrupting calibration returns control to you, but the PMM will not be calibrated.

You can also calibrate the PMM from within your test program. Use the `set pmm cal_mode` statement to tell the PMM which autocalibration routine or routines to run:

```
set pmm cal_mode: dc; /* run the DCV routine */
set pmm cal_mode: ac; /* run the ACV routine */
set pmm cal_mode: ohms; /* run the OHMS routine */
set pmm cal_mode: all; /* run all the routines */
```

Alternatively, specify a combination of routines by enclosing them in parentheses separated by spaces. For example:

```
set pmm cal_mode: (dc ac); /* run DCV and ACV */
```

Then use the `set pmm cal` statement to tell PMM when to run the autocalibration routines you selected. The choices are:

```
set pmm cal: off; /* Do not run them */
set pmm cal: once; /* Run them when a "set pmm" */
                   /* statement is executed          */
set pmm cal: on;   /* Run them on a regular basis, */
                    /* usually every four hours. */
```

Normally, autocalibration information is bundled into a single `set pmm` statement, such as:

```
set pmm
cal_mode: all
cal: once;
```

Calibrate the meter when absolute accuracy is necessary. Calibrate all PMM modes once every 24 hours. Use the function `tl_pmm_dump_cal_times` to determine the time of the last calibration for `dc`, `ac`, and `ohms`.

Advanced Time Measurement Subsystem (ATMS)

Calibrate the advanced time measurement subsystem (ATMS) by using the command

```
calibrate [-station#] -tms
```

This command calibrates the:

- Interpolators
- Local clock
- Threshold D/A converters
- Input channel path lengths

To perform full calibration on the ATMS from within a test program, run DC calibration using the following statement:

```
start tms: cal_full;
```

Use the following statement to calibrate only the interpolators and local clock:

```
start tms: cal;
```

If calibration fails, you must recalibrate or initialize your test system. To initialize your test system, select Initialize from the IMAGE gray-area pop-up menu or type `initialize` in a station window. This command returns all ATMS calibration values to their defaults.

Precision Low-Frequency Digitizer (PLFD)

The most efficient method of precision low-frequency digitizer (PLFD) autocalibration is to let IMAGE do it automatically at regular time intervals. This method is known as autocalibration. To activate autocalibration, simply include the `autocal` switch when loading your test program. In the station window, type

```
load -autocal <file name>
```

where `<file name>` is the name of your test program. Once autocalibration is activated, IMAGE automatically calibrates the PLFD every 4 hours. Use the `tl_plfd_cal_interval()` function to change the calibration interval from 4 hours to some other time interval. For example, the following function call changes the calibration time interval for all PLFDs to 8 hours:

```
tl_plfd_cal_interval(60*60*8);(interval units
are seconds)
```

To calibrate a PLFD from within your test program, execute the following ITL statement:

```
start plfdig: cal;
```

To calibrate a specific PLFD channel card, use

```
start pin=<pin_spec> plfdig: cal;
```

To calibrate all PLFDs in the tester, enter the following command in a station window:

```
calibrate [-station #] -plfdig
```

Precision-Low Frequency Source (PLFS)

Precision low-frequency sources (PLFSs) must be calibrated. Use one of the following statements or autocalibration. An attempt to start sourcing an uncalibrated PLFS results in a run-time error.

Calibrate the PLFS using the command `calibrate [-station #] -plfsrc` where `-station #` specifies the test station for PLFS calibration, and `-plfsrc` is the switch for PLFS calibration.

You can also calibrate the PLFS from within a test program. Start calibration using the statements `start <pin ID> plfsrc: cal;` and `start plfsrc:cal;` where `<pin ID>` is a constant, a pin number, a pin name, a pin list, a variable, or a field.

These statements initiate calibration of the AC linearity of the PLFS digital-to-analog converter.

This routine takes about 30 seconds and is executed when you power up the test system and load a test program for the first time. It also happens each time autocalibration is run. Subsequent program loads do not require recalibration.

Very High-Frequency Arbitrary Waveform Generator (VHFAWG)

The VHFAWG instruments (VHFAWG -> VHFAWG1200) must be calibrated to maintain fine attenuation linearity and absolute level accuracy specifications. Use IMAGE to automatically calibrate the VHFAWG and the test system by using the `-autocal` switch when you load your test program.

The `-autocal` switch causes IMAGE to automatically calibrate the VHFAWG instruments and the test system after the first run, provided the test system passed calibration during the first run of the test program. IMAGE monitors the temperature and recalibrates the VHFAWG if the temperature variation is outside the specifications.

The calibration data for the test system is updated after each calibration. If you do not use the `-autocal` switch, your test program must calibrate the VHFAWG instruments and the test system at the proper intervals to maintain test system specifications.

If you enable autocalibration, change the interval between calibrations with the following function. `Time` is the interval in seconds between calibration runs.

```
tl_vhfawg_cal_interval(time)
```

If you do not enable autocalibration, calibrate the VHFAWG by using one of the following three methods:

- Type the following command in the station window to immediately calibrate all VHFAWG in the test system regardless of the last calibration:

  ```
  calibrate -vhfawg
  ```

- To calibrate all VHFAWG in the test system:

  ```
  start vhfawg: cal;
  ```

- To calibrate a specified VHFAWG in the test system, `pin ID` is the pin connected to the VHFAWG that you want to calibrate. The default VHFAWG for a pin is the VHFAWG assigned to the pin as a channel in the pinmap.

  ```
  start pin=<pin ID> vhfawg: cal;
  ```

Very High Frequency Continuous Wave (VHFCW) Source

Calibrate all very high-frequency continuous wave (VHFCW) sources in the test system using the command `calibrate [-station #] -vhfcw` where `-station #` specifies the test station for VHFCW calibration and `-vhfcw` is the switch for VHFCW calibration.

If you load a test program in IMAGE V4.0 or higher using the `-autocal` option to the `load` command, all VHFCW calibration is performed automatically.

To calibrate the VHFCW from within your test program, use:

```
start pin = <pin ID> vhfcw: cal;
```

The above statement starts calibration for the default VHFCW source assigned to each pin in the `<pin ID>`. The default VHFCW source for a pin is the VHFCW source assigned to the pin as a channel in the pinmap.

The following statement starts calibration for the VHFCW source and channel specified:

```
start slot = <int> schan = <1 | 2> vhfcw: cal;
```

The following statement starts calibration for all VHFCW sources in the test head:

```
start vhfcw: cal;
```

High-Speed Sampler (HSS)

To calibrate the High Speed Sampler (HSS) use the following function call:

```
tl_hfsc_ramp_cal();
```

This function inspects the sampler timing and generates a table of calibration constants. The sampler uses the calibration constants to improve the accuracy of the `strobe_delay` for step and fixed modes of operation. In sweep mode, the sampler uses the calibration constants to improve the accuracy of sample-to-sample timing.

Note

You must calibrate the time measurement subsystem and the DC subsystem before calibrating the sampler.

High Current Unit (HCU)

The high-current unit (HCU) calibration is performed in the DC subsystem calibration. Refer to Section DC Subsystem for information on the DC subsystem calibration.

High-Speed Digital (HSD) Channels

IMAGE automatically calibrates the test system using the `-autocal` switch when the test program is loaded. The `-autocal` switch causes IMAGE to automatically calibrate the test system as needed after the first run (if the test system passed the test).

IMAGE repeats the calibration when the temperature changes more than 3°C (37.4°F) or if it recognizes a change in the high speed digital (HSD) subsystem. The calibration data for the test system is updated after each calibration. If you do not use the `-autocal` switch, the test program must calibrate and deskew the test system at the proper intervals to maintain test system specifications.

cal_set statement

Specify and execute a calibration set at least once at the beginning of the test program, using the `cal_set` statements described in this section. The `cal_set` statement causes IMAGE to calibrate the following components sequentially:

- aDC calibration: Calibrates A/D on the LA670 CSB
- pwrsrc calibration: Test head programmable power supply calibration
- HSD levels as specified in the `cal_set` statement or to default values if voltage levels are not specified
- HSD timing edges for all formats

If calibration is successful, IMAGE creates a set of calibration data for all channels in the CALSET. If a channel fails calibration, the test program stops. If you selected `continue on fail` the test program uses the default calibration values and continues.

Calibrate the HSD subsystem at the voltage levels that you plan to use in your test program to achieve the specified timing accuracy.

For more detailed information about the HSD subsystem calibration, refer to the IMAGE Base Language Reference Manual (pn 553-403-17).

cal_set Syntax

```
set hsd cal_set = "<setname>"
vrange: <rangespec>
[ppmu_vsys = <value>]
[dut: open | closed]
```

```
pin = (1 to xxx)
vih = 2.5v
vil = 0.5
voh = 2.5
vol = 0.5
ioh = -10 Ma
iol = 25ma
vcp = 2.5v
ppmu_v_force= 0.5
ppmu_v_meter= 0.5
ppmu_i_force_2ma= 2ma
ppmu_i_force_200ua= 200ua
ppmu_i_force_20ua= 20ua
ppmu_i_meter_2ma= 2ma
ppmu_i_meter_200ua= 200ua
ppmu_i_meter_2ua= 2ua
ppmu i meter 200na= 200na
```

Where `rangespec` is one of the voltage ranges: `high` | `middle` | `low`. The default is `high`.

`value is the systemwide voltage at which the PPMU is to be calibrated. The voltage can be from -4.0V to +7.0V depending on voltage range. If no ppmu_vsys <value> is specified, the default values depend on the range as shown below:`

Table 1:

vrange	ppmu_vsys
high	5.0V
middle	4.0V
low	3.0V

`dut` is the DUT relay on the HSD channel card. The choices are open and closed. The default is open. When the DUT relay is open, the channels are calibrated up to the DUT relay. The calibration signals and voltages are not applied to the DUT pin to prevent DIB circuitry or device loading from causing calibration to fail. When the DUT relay is closed, the channels are deskewed up to the DUT pin connection.

Note

The DUT relay can be programmed open if circuitry on the DIB interferes with the TDR path length measurements, or if the DUT is in the socket when calibration is performed. Autocalibration via the `cal_set` statement automatically opens the DUT relay when recalibration is executed.

`target` is the level on the waveform at which deskew is performed. The range is from 20% to 80%. The default is 50%.

Calibration failure is frequently caused by hardware failure. System checkers should be used to determine the source of any failures that occur.

To execute the `cal_set` from within the test program use the following statement below:

```
start hsd cal_set= "<setname>";
```

To immediately calibrate and deskew the test system and all channels present to the default values, type the following statement:

```
calibrate -hsd
```

Internal/External System Checkers (Level 2)

System Check

The table System Check Programs lists all the checkers that are executed in full and brief modes of system check, as of IMAGE Version 6.3. The list changes depending on system configuration. The main difference between full and brief mode is that some sequencers are run in brief mode. This causes fewer tests to be executed.

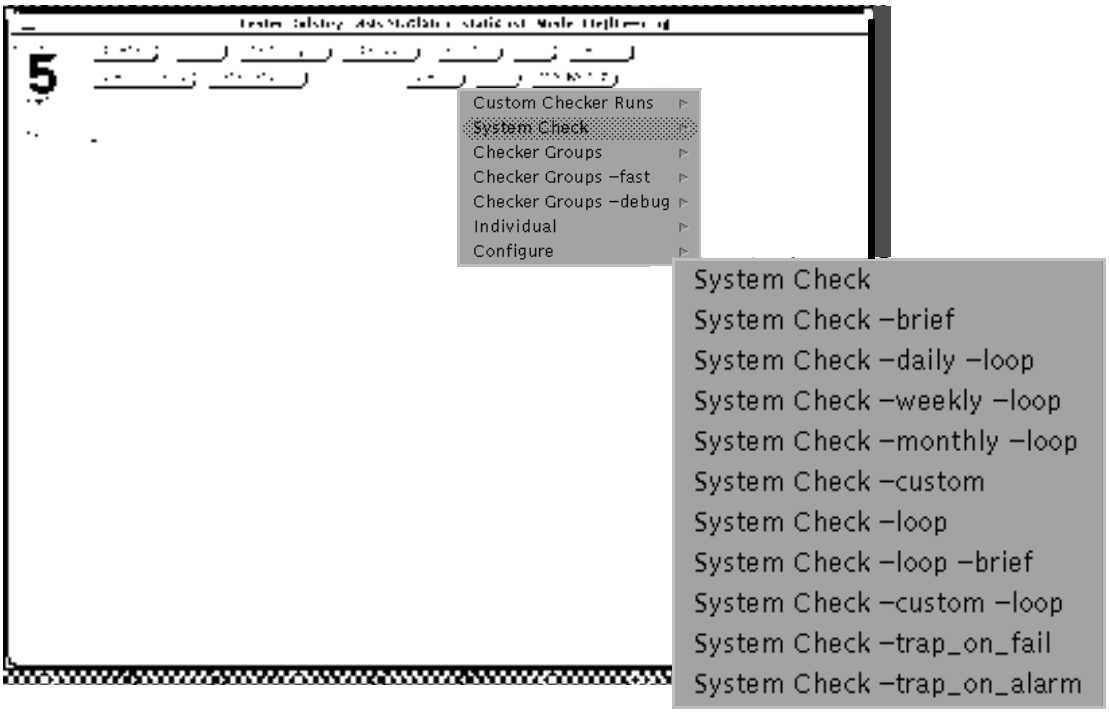
Common_frame_ck group	Catalyst_head_ck group
databus	headst
ubst	ubasyst
dcst	tmsalst
matrixst	pmmst
stationst	trgst
ubapust	tmemdlyst
apust	hsd_st
asyst	tjdst
hcust	pacsII_ams_st
ovist	hfsampalst
apxferlinst	vhfcwst
	vhfst
	vhf_am_st
	plfalst
	plf_ams_st
	lfacst
	lfac_ams_st
	modscrst
	uwst

System Check Procedure

Use this procedure to run the full complement of checkers with the exception of the mi and CV checkers.

1) Verify that the test system power is on. Log in to the system as **`checkers`**.
2) Invoke the IMAGE program by entering the command **`image`**.
3) Log in to Station 5 as **`checkers`**.
4) Move the mouse pointer to the top section of the station window. Place the pointer on the checkers selection and press the right mouse button.
5) Move the mouse pointer slowly downward until **`System Check`** is highlighted.

6) Move the mouse pointer slowly toward the right until a menu selection appears and **`System Check`** is highlighted. Refer to the figure System Check Submenu. Release the mouse button to load and run the checker. Moving the mouse pointer until **`System Check-brief`** is highlighted loads and runs checkers in brief mode.



System Check Submenu

catalyst_continuity_mi Procedure

Equipment Required

For catalyst_continuity_mi, the continuity DIB (pn 805-761-00) is needed. This is in the checker tool kit (pn 806-166-05).

Load and Run catalyst_continuity_mi

The console window must be open to view error messages.

1) Install the DIB (pn 805-761-00) onto the test head.
2) Verify that the continuity jumper block area (W1, W2) in the center of the DIB is fully populated.
3) Move the mouse arrow to the top section of the station window. Place the arrow on CHECKERS and press the right mouse button.
4) Move the mouse slowly downward until *Individual* is highlighted.

5) Move the mouse slowly towards the right until a menu selection appears and then slowly downward until *Maintenance and Installation* is highlighted.

6) Move the mouse slowly towards the right until a menu selection appears and then slowly downward until *catalyst_continuity_mi* is highlighted. Release the mouse button. The checker then loads into the station window.

7) Move the mouse arrow to the top section of the station window. Place the arrow on top of the RUN selection and press the left mouse button. Checkers now runs.

Monitor the console window for error messages.

External Calibration for Internal References (Level 3)

Reference Calibration Overview (AD412 Board)

The AD412 calibration reference board is the internal system calibration card for Catalyst. It contains precise voltage and resistance standards for use in calibrating the DC subsystem and other hardware in the test system. Overall DC subsystem accuracy and traceability are derived from this reference.

The AD412 reference achieves absolute accuracy by using a 2K x 8-bit nonvolatile EEPROM to store any measurable offsets of the various voltage and resistance references as measured with an external traceable standard.

IMAGE linear regression algorithms calculate the appropriate gain and offset terms from actual measurements on the hardware. Reference error data stored in the EEPROM is also used. The correction terms are digitally applied to DACs on the individual AD204 source control boards to adjust the output of the source for the greatest accuracy on a given range. The voltmeter corrections are applied to the raw A/D value read after a measurement. The data is stored in the EEPROM using Teradyne's supplied procedures and an external DVM.

The AD412 is accessed internally through matrix pins 1, 2, and 3, or externally via J3 or J4 (20-pin connectors on the flipper edge of the board).

The AD412 has other circuitry to allow connection of nonmatrix V/I sources to matrix pins 1 and 3. These DC sources can now be calibrated since they can be connected to the matrix much like the other matrix sources.

An ID PROM is provided to store the standard information about the board. Board number, serial number, and revision date are encoded and can be read back by the software as a serial number for the board. This is one of many requirements of traceability to national standards.

Voltage References

The voltage references are derived from a 6.95V heated zener reference. Amplification and inversion provide ±10V that is used as the main board reference. A number of various gains are applied to the main reference to provide the proper output voltages. The voltage references are available under software control to the test system on matrix pin 1.

Resistor References

The resistor references are made up of high-precision resistors. They are switched in and out with relays and are arranged in a four-wire kelvin configuration. The low side of the resistors is connected to ground, although a provision is made to allow for nongrounded operation. During DC subsystem calibration, current flowing through the resistor (HF to LF) produced by the V/I source generates a voltage across the resistor proportional to the current. This current can be accurately measured via the sense connections with a voltmeter.

The AD412 has an extra safety feature: An automatic shutoff circuit removes the resistor from the matrix pins after a predetermined time of approximately 10 ms to prevent excess power dissipation. The resistance standards are available to the test system on matrix pin 3 (to ground). Matrix pin 2 is used as an LF/LS connection when making external measurements to reduce system ground errors from affecting the measurement.

External Connections

Two 20-pin connectors on the flipper end of the board (J3 and J4) are used to program the voltage and resistance references to other instrumentation in the system for calibration purposes. The external connectors J3 and J4 are daisy-chained and are active when programmed to external mode. Internal connections to the matrix and external connections cannot be selected simultaneously.

Checker Execution

Checkers may require a password. If so, contact the system administrator to obtain it.

Equipment and Setup for dcrefcal

DCREFCAL is used to measure and store the errors associated with the AD412 voltage and resistance references. DCREFCAL is used in the Catalyst IMAGE environment.

The errors found at each reference voltage and resistance are stored in an EEPROM on the AD412 board. The DC calibrator can use the reference corrections to provide accurate DC references.

When a system is shipped from the factory, the dcrefcal constants are set to zero and the system is verified to meet specifications at this setting.

Equipment Required

Qty	Model	Description
1	HP 3458A-002	Digital Multimeter with High Stability Reference
From the Base Reference CAL Tool Kit (pn 803-800-00):		
2	358-216-04	BNC Test Cable Assembly
2	358-692-00	Adapter BNC Jack to Banana
1	901-258-00	Alligator to Banana

Required Catalyst System Configuration

Matrix pins 1 through 3 and the AD412 reference board are required to run *dcrefcal*.

Note

This procedure assumes the Catalyst system is running IMAGE software. To stabilize the reference, system power must be on continuously for 30 minutes (with all system covers closed) before executing this procedure.

Standards Verification Connection

Two BNC connectors labeled J4 OHMS and J5 VOLTS are located on the central plate on the front of the Catalyst mainframe cabinet.

HP 3458A Meter Setup and Calibration

Autocalibrate the HP 3458A meter. The HP 3458A must undergo autocalibration every 24 hours.

1) Disconnect any leads to the meter.
2) Press the auto_cal key, then the up arrow key. This calibrates ALL modes.
3) Press the Enter key to begin. This takes approximately 11 minutes. Do not make any connections to the meter until the process is complete.

The meter can be programmed with a password.

If running over IEEE, connect the meter to the IEEE interface. Set the meter address to 10. Instructions on how to set the meter address can be found in the HP 3458A manual.

If running manually, set the meter as follows:

1) Turn OFFSET COMP ON.
   -Press OFFSET COMP, up arrow, then Enter.

2) Set NPLC to 30.
-Press NPLC, 30, then Enter.

3) Set to DC voltage for voltage verification measurements.
When testing resistance, switch to OHMF (blue button).

Connect the HP meter to the standards verification BNC connectors on the system. Refer to figure DCREFCAL DVM Connections.

- Meter input to J5 volts
- Meter ohms to J4 ohms
- Meter guard to system ground (Refer to the section dcrefcal Procedure, step 11).

dcrefcal Procedure

1) Log in to a station window as **checkers**.
2) Right click the CHECKERS button. Then right-click Individual, Maintenance and Installation, and dcrefcal.
3) Using the right mouse button, set the termination mode under the RUN button to “continue on error”.

Invoke the checker by typing **`run`** and pressing **`<return>.`**

4) A statement with the revision date of the checker appears, along with a statement displaying the AD212 or AD412 serial number. Respond with `y` and press `<return>.`
5) The next message displayed is an overall summary message on the checker. It states which meter can be selected for remote operation (IEEE). This differs, depending upon the revision of the checker. Press `<return>.`
6) The main menu is then displayed. Respond with `1` and press `<return>` to collect a new set of correction data. This selection does not change the data stored on the AD412.
7) Displays may vary at this point, depending upon the revision of the checker. Answer the questions appropriately.
8) Before answering the question regarding communicating via the IEEE, the meter must be connected. If `y` is the response to the question to communicate via the IEEE interface, respond with `2`, since only the HP 3458 supports Catalyst specifications.
9) After responding with `2` to question 9, the following setup message is displayed. See figure Calibration Setup Message.

```
Before calibrating references, THREE connections must be made
between the meter and the STANDARDS VERIFICATION jack.

Connect the DVM voltage inputs to the jack labeled
"Volts".

Connect the DVM ohm inputs to the jacks labeled "OHMS".

Connect the DVM GUARD input to systems ground.

Make sure the guard button is set to "OPEN"
(not depressed).

The HP listen address must be set to decimal "10".

Hit RETURN to continue=>
```

Calibration Setup Message

10) Connect the meter before pressing `<return>`. A suitable system ground connection is obtained by connecting the alligator clip to one of the cable sock retaining hooks. The hooks are located below the standards verification panel and underneath the VELCRO closure. See figure DCREFCAL DVM Connections.

11) If the response was `y` press `<return>`. If the meter has been connected properly to the IEEE interface, the voltage verification measurements are made first, followed by the resistances. If the IEEE bus is not being used, enter the readings manually. When entering the measurement results manually, include the decimal point.

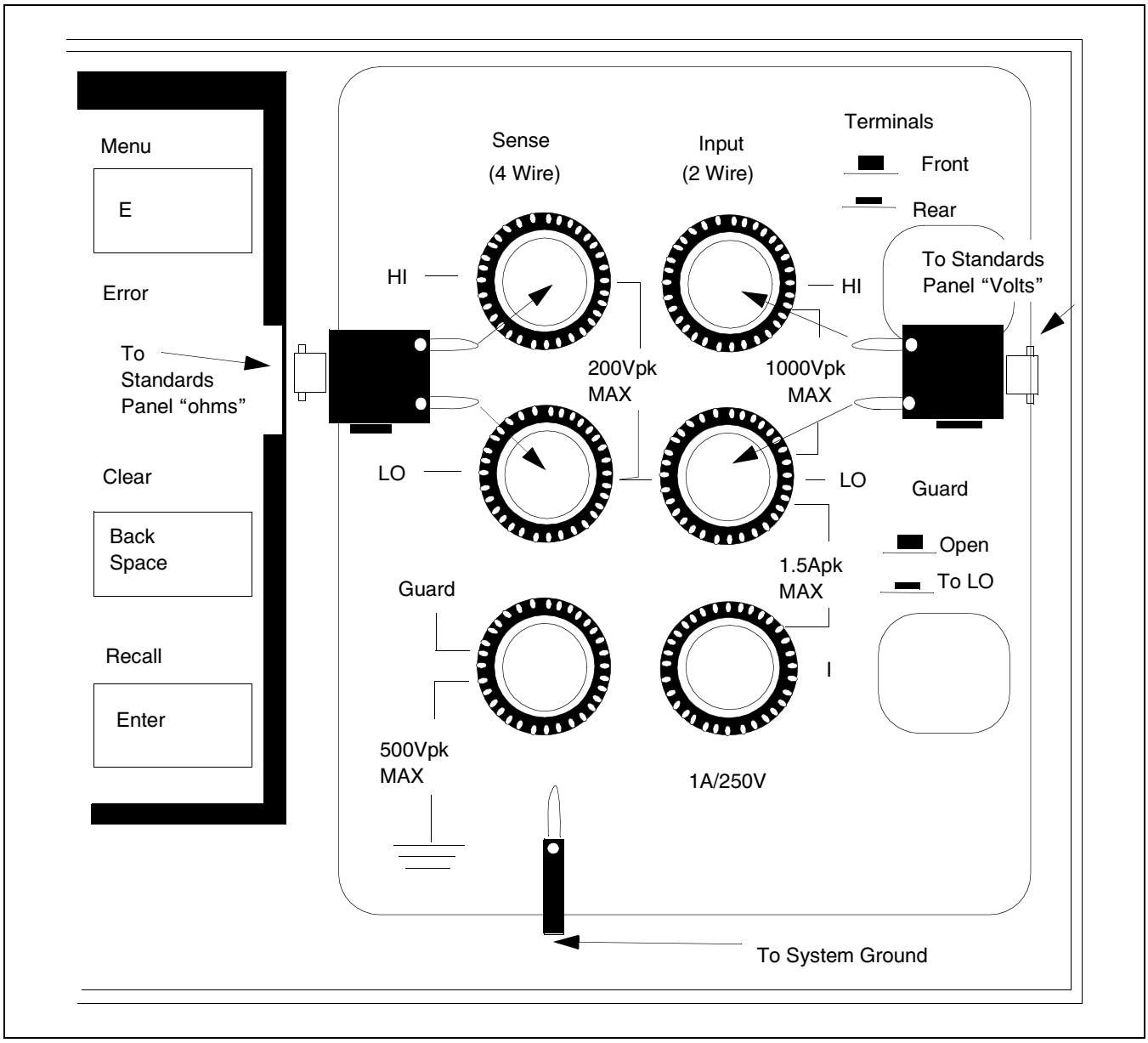
12) The last resistance measurement to be verified is 50 ohms. After completing this measurement, manually or via the IEEE bus, an example of the table is displayed. If all the readings in the table pass, enter `y` and press `<return>`. To record the constants as the current table. If any failures exist, respond with `n` and press `<return>`. Failures are indicated by `*F`.

13) The main menu is displayed. If failures occurred in the previous step and `n` was the response, type `0` to exit the menu level and troubleshoot the problem. If `y` was the response, enter menu selection `2-Save the current table`. This saves the current table on the AD412 EEPROM.

14) Enter menu selection `6`, Data retention verification. Ensure data retention is verified.

15) Enter menu selection `4`, Create file of all stored tables. This creates a file called “DCREF_HISTORY” which is stored in the current working directory.

16) Type `0` to exit the program. The program must pass a BIN 1.



DCREFCAL DVM Connections

LA703-00 10/100 MHz Crystal Oscillator Overview

The LA703-00 10/100 MHz reference and distribution module uses an oven-controlled crystal oscillator (OCXO) (10 MHz standard) to generate 10 MHz and 100 MHz reference signals. These signals are distributed throughout the tester for use as references to the PTS synthesizer, PACS II card cages, digital card cages, the time measurement system (TMS), and the trigger bus.

The 10/100 MHz reference signals provide a 10 MHz and a 100 MHz reference for time and frequency synchronization. The 10 MHz reference is used for calibrating all synchronous systems resources such as the synthesizer generators, the TMS, the trigger switchyard (TSY), and the UHF instrumentation options. The 100 MHz reference is used for the Catalyst digital subsystem and PACS subsystem.

The LA703-00 100 MHz master clock reference is coherent with the 10 MHz reference source and has low phase noise, minimum time jitter, low skew, and high stability. The 100 MHz reference can be enabled or disabled by a signal sent out by the LA620-00 BIF data interface board.

The LA703-00 10/100 MHz reference module is mounted in the upper left section of the service side, above the computer card cage.

10 MHz Reference Oscillator

The 10 MHz OCXO has excellent temperature stability and phase noise performance that exceeds synthesizer specifications. Using the crystal bandpass filter inside the synthesizer's 10 MHz path further improves the phase noise performance for UHF instrumentation.

10 MHz External Input

The external input can be used either to couple the onboard 10 MHz OCXO into the reference board, or the user can connect his own 10 MHz reference oscillator with a >7 dBm, sine, 50Ω termination to the external 10 MHz input, which then becomes the reference.

Reference Distribution Circuitry

An SMA connector is provided for access to the direct output of the OCXO. Normally, an external jumper cable is used to connect the OCXO output to the external input. When using an external 10 MHz signal connect the signal to the external input instead of the jumper.

At the input there is a 2 dB attenuator pad that is used to correct the level at the sine outputs and to provide a 50Ω input impedance.

Following the 2 dB pad, two amplifiers are used to buffer two separate signal paths. One path has three parallel buffers to provide the sine outputs, and the other path is used to convert the sine signal to three differential ECL outputs. An RF transformer is used to provide isolation between the system's digital and analog grounds.

X10 Phase Lock Loop

The phase lock loop (PLL) takes the 10 MHz output signal and increases it to 100 MHz while maintaining the accuracy and stability of the 10 MHz crystal. The X10 PLL is made up of an input divider, phase detector, loop low pass filter, VCXO, and a feedback divider. The combination of input and feedback divide ratios results in a gain of 10. The phase detector is filtered by a low pass filter to get the DC component of the phase detector output. The result is a 100 MHz output that meets the performance of a crystal oscillator.

100 MHz External/Internal Jumper

The LA703-00 provides for selection of an external or internal source for the 100 MHz signal. Normally, an external coaxial jumper is installed that connects the internal 100 MHz signal to the rest of the output chain. However, this jumper arrangement allows for an external 75 to 100 MHz sine wave signal to be fed into the bandpass filter (BPF).

Sine/LVPECL Conversion

The output of the 100 MHz BPF, which is sinusoidal, must be converted to low-voltage positive-supply ECL levels (LVPECL). This is accomplished with the use of a wide-band amplifier to maximize slew rate. AC coupling is then used to route that output into the differential inputs of an LVPECL device.

100 MHz Clock Distribution

The 100 MHz clock signal CLK100 is distributed to clients via differential LVPECL drivers. These drivers are within the same IC, which is designed specifically for clock distribution (having guaranteed skew performance plus the ability to be enabled synchronously). The enabling signal is issued by the CPU via the BIF. Access to the CLK100 signals is via 3-pin headers compatible with 50Ω shielded 2-conductor cables. In addition, a sine output is provided via an SMA connector for potential use by a future RF/microwave instrument, as well as serving as a test port.

LA703 10 MHz Master Reference Module Calibration Setup

This procedure is used to verify the LA703 frequency accuracy specification.

The LA703 is the frequency/time standard in the Catalyst test system. All PTS synthesizers are frequency locked to the LA703 10 MHz master reference module and do not require separate calibration.

Equipment Required

Qty	Model	Description
1	HP 5313A-010	The timer counter used for this calibration must have been calibrated within three weeks of its use in this procedure. An equivalent timer counter can be used if the frequency accuracy at the time of test is better than 0.2 Hz at 10 MHz.
From the Catalyst Level III CAL Tool Kit (pn 803-800-00):		
1	358-216-04	BNC Test Cable Assembly

Checker Execution

The LA703 and HP 53131A must be powered on for at least 30 minutes before performing this procedure.

The LA703 module is located in the upper left corner, service side, of the Catalyst mainframe. For convenience, the 10 MHz and 100 MHz frequency references are brought out to the connection points on the service side EMO panel. See figure Catalyst Mainframe Service Side for information relative to the location of the LA703 and its interfaces.

Automatic Counter Control and Data Collection Method

The LA703 calibration procedure can be done manually or via IEEE interface. If the IEEE interface method is chosen, load and run the freq_ref_mi.load program. In IMAGE Version 6.3 and later, the file can be found in the $CKRBIN directory. For instances where IMAGE versions earlier than 6.3 are in use, the freq_ref_mi.load program is provided with Level IV program release tape.

Follow the instructions provided by the program. The program must pass BIN 1. if adjustment of the reference oscillator is required, the program instructs the operator to adjust the counter. To accomplish this, follow the LA703 adjustment procedure in section LA703 Adjustment Procedure.

The counter is placed in continuous measurement mode by the test program during the adjustment period to facilitate the proper adjustment.

Manual Calibration Method

10 MHz REF CAL

Connect a BNC cable from the EMO panel 10 MHz output to channel 1 on the counter.

Perform the following key sequence:

1) Frequency and Ratio
2) Gate and Ext Arm (twice)
3) Adjust gate time to one second. Use the arrows to the right of the display.
4) Press the ENTER button near the arrows to confirm the gate time.
5) Frequency and Ratio
   - The counter displays 10 MHz with the appropriate accuracy.
   - The counter must display 10 MHz ± 3.0 Hz for the LA703 to meet system specifications.
   - The LA703 must be adjusted if the counter displays an output not within 10 MHz ± 0.5Hz. This will guarantee that the LA703 will remain within specification for the next year.
   - If the LA703 requires adjustment, follow the instructions in section Section LA703 Adjustment Procedure.

100 MHz Reference Verification

The 100 MHz reference output is created from the 10 MHz signal.

1) Connect the 100 MHz output to the channel 1 input on the counter.
2) Connect the 10 MHz output on the EMO panel (J8) to the external reference input of the HP 53131A (located on the rear panel).
3) The counter display MUST indicate 100 MHz ± 0.1Hz.

Note

The 100 MHz output is a direct product of the 10 MHz output (multiplied by 10). This relationship is verified by using the LA703 10 MHz output as the timebase reference input to the HP 53131A and measuring the 100 MHz output.

LA703 Adjustment Procedure

The adjustment of the LA703 oscillator reference is accomplished via an adjustment screw located on the right side of the LA703 module. The screw is accessed by removing the plastic exterior screw on the oscillator case.

Due to the location of the screw an access hole is provided in the top rear mainframe bar. A special longhandled nonconductive screwdriver has been supplied. The screwdriver is located below the 10 MHz and 100 MHz outputs on the service side EMO panel.

1) Remove the plastic screw.

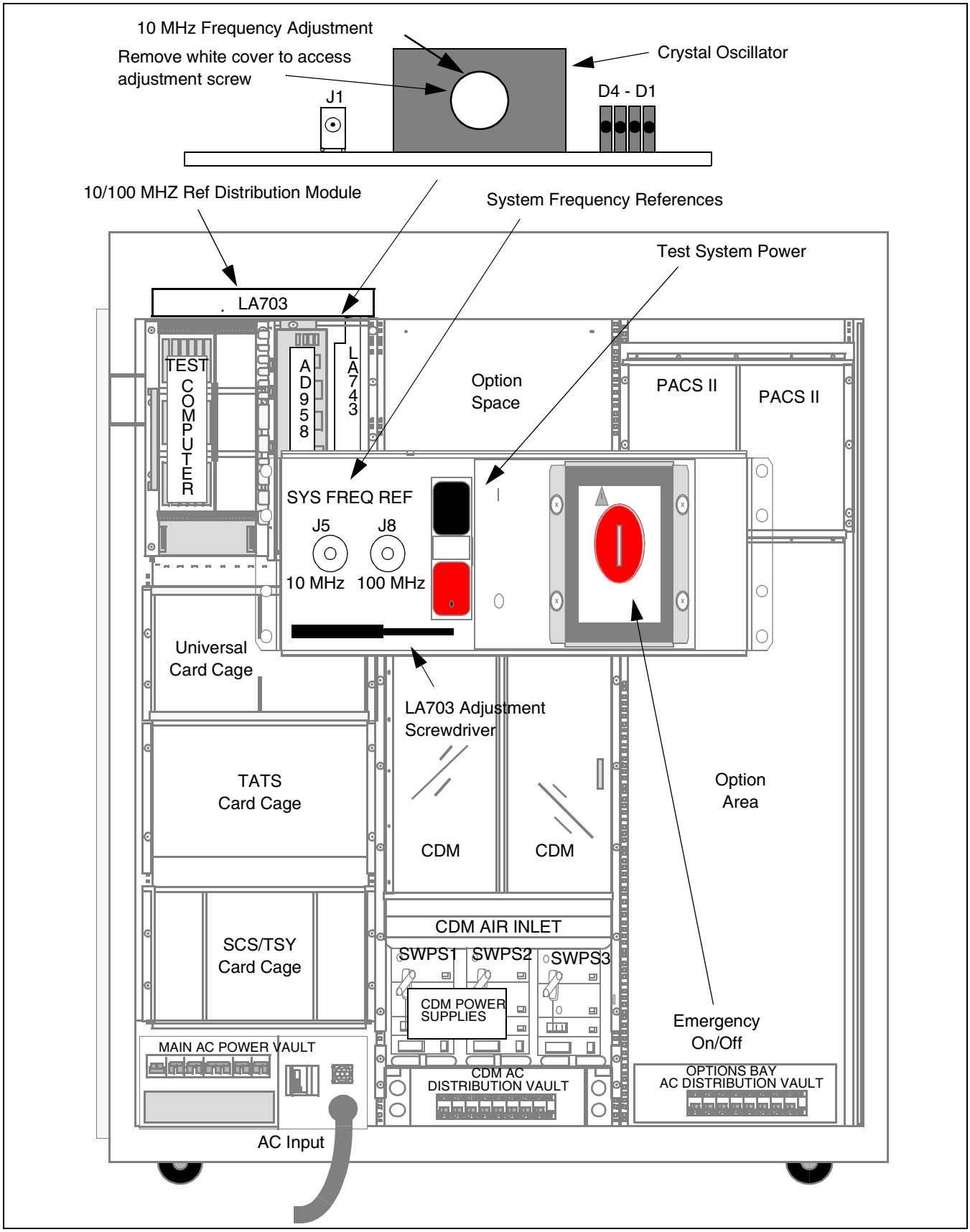
2) Adjust the screw clockwise if the frequency is too high. Adjust the screw counterclockwise if the frequency is too low. DO NOT turn the screw more than 1/4 turn without verifying the change at the counter.

3) Replace the plastic screw. Replacing the screw is important because the cover allows the oscillator to maintain proper temperature regulation. Hand-tighten the screw. Do not overtighten.

4) Verify the 10 MHz output a final time. If you are running the automated process, the program performs this task.

Note

Once the HP 53131A counter is placed in external reference mode, it is necessary to reset the counter to its internal reference. Do this by cycling the ON/OFF button on the front panel of the counter. The manual reference calibration can then be repeated. The automated (IEEE) version of this procedure does not require this action because of a slightly different test implementation.



Catalyst Mainframe Service Side

Equipment and Setup for hcurefcal

The hcurefcal checker measures and stores the errors associated with the HCU internal resistance references on the TJ151-00 board. The error found at each reference resistance is stored in a file that resides in /image/tester/<host name>/cal. These reference corrections can then be used by the HCU calibrator to provide accurate HCU references.

Equipment Required

Qty	Model	Description
1	HP 3458A	Digital Multimeter
From the Catalyst Level III CAL Tool Kit (pn 803-800-00):		
1	804-096-00	CBL, HCU REF CAL

Setup

HP 3458A meter:

Autocalibrate the HP 3458A meter. The HP 3458A must have been autocalibrated within 24 hours. The meter may be programmed with a password.

1) Disconnect any leads to the meter.
2) Press auto cal button, then the up arrow button.
   This calibrates ALL modes.
3) Press the Enter button to begin. This takes approximately 11 minutes. *DO NOT* make any connections to the meter until the process is complete.

Connect the test cable (pn 804-096-00) from the HP meter to the REF1 and REF2 jacks. These are located near the DC standards connectors on the standards verification panel.

- Sense High and Input High Shield to REF1
- Sense Lo and Input Lo Shield to REF2
- Meter guard to system ground (Refer to section dcrefcal Procedure, step 11)

If running over IEEE, connect the meter to the IEEE interface. Set the meter address to 10. Instructions on how to set the meter address can be found in the HP 3458A meter manual.

If running manually, set the meter as follows:

1) Turn OFFSET COMP ON.
   Press OFFSET COMP, up arrow, then Enter.

2) Set NPLC to 30.
Press NPLC, 30, then Enter.

3) Set the switch to OHMF (blue button) for resistance verification.

hcurefcal Procedure

1) Log in to a station window as **checkers**. You may need a password.

2) Load the hcurefcal checker by one of two methods:

   - Right-click the checkers menu to load the checker listed under the Individual - Maintenance and Installation menu.
   - Type **load $CKRBIN/hcurefcal.load** at the station window prompt.

3) Set the termination mode under the RUN button to "Continue on error".

4) Run the checker by typing **`run`** and pressing `<return>`.

5) Follow the instructions provided and answer the questions in the following menus.

6) At the command menu, enter `1` and press `<return>`.

7) Displays may vary at this point, depending on the revision of the checker. Answer the questions appropriately. Before answering the questions regarding communication via the IEEE interface, the meter must be connected. If the answer is `y press <return.` The meter selection and setup are displayed.

8) Connect the meter as stated in the section Setup above, before pressing `<return>`.

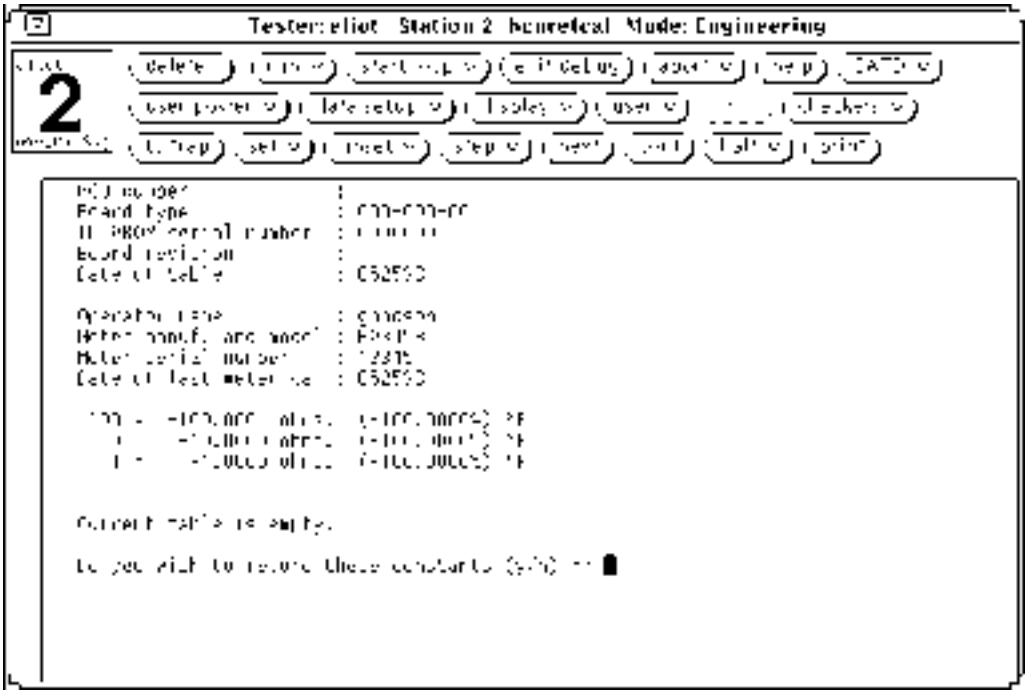
9) If the response was `y` press `<return>` to the question regarding communicating using the IEEE bus, and the meter has been connected properly, the resistance verification measurements are performed. If the IEEE bus is not being used, enter the readings manually. When typing in the measurements manually, include the decimal point.

10) The last resistance measurement to be verified is the 1 Ω measurement. Upon completing this measurement (whether manually or via the IEEE bus) **IF** all the readings in the table pass, then enter `y` and press `<return>.` This records the constants as the current table. If any failures exist, enter `n` and press `<return>.` Failures are identified by `*F`.

11) The main menu is displayed again. If any failures had occurred in the previous step, enter `0` to exit menu level and troubleshoot the problem. Check the meter selection and setup before replacing the TJ151-00. If y was the response the current table was stored in the errorlog file named hcu_refcal.log, which resides in the /image/tester/<host name>/cal directory. The stored table is used in the HCU calibrator and checker.

12) The hcu_refcal.log file holds measured reference error data, but this data should be used only for the referenced HCU board. So, if that board is changed, the logged data becomes useless. In that case, enter menu selection 3 to erase data. After the selection, the confirmation message is displayed. If you really want to erase the logged data, enter `y` and press `<return>`. Otherwise, enter `n` and press `<return>` or just press `<return>`.

13) Type `0` to exit the program. The program must pass a BIN 1.



Current Constants Menu Display

Overview of pmm_xcal_mi

The PMM calibration process consists of two parts: DC calibration and AC calibration. The DC calibration is performed inside the system. For an explanation refer to an overview of DC calibration. An alternate DC calibration method can be performed outside of the system in a qualified calibration lab with certain considerations. Refer to section Alternate DC Calibration.

AC calibration can be performed only outside of the system in a qualified calibration lab.

To achieve the highest level of DC performance, Teradyne recommends performing DC calibration every 90 days. It is also recommended that AC calibration be performed every two years.

The following sections describe how to run the pmm_xcal_mi program.

Before running pmm_xcal_mi, the system's internal environment must be stable for 4 hours. This means that test system power must be on and all covers in place for 4 hours before running this program.

The pmm_xcal_mi program is loaded from the checker menu. The entire program takes about 30 minutes to complete. It does not produce a datalog output file. It does produce a pmm_xcal_record file, which contains information about the calibration process. This file is stored in the current working directory; if the current working directory already contains a pmm_xcal_record file, the results of the new file are appended to the existing file. The pmm_xcal_record file contains:

- The operator's name
- The model name, serial number and calibration date of the 10V standard used during the calibration process
- The name, serial number and calibration date of the 10K standard used during the calibration process
- The offset voltage and resistance of the PMM input path
- The entered values of the external 10V and 10K references

The program operates in the following sequence:

- Information is collected regarding the equipment used.
- The jumper cable connections are checked for proper hook-up.
- The PMM input path's offset voltage and resistance are measured.
- The meter's internal DC voltage standard is calibrated using the external 10V reference and a DC autocalibration is performed.
- The meter's internal resistance standard is calibrated using the external 10K reference and an ohms autocalibration is performed.
- An AC autocalibration is performed:

At the end of the program, the PMM’s internal DC voltage and resistance references have been externally calibrated and the PMM has been autocalibrated.

After each connection setup the program waits 5 minutes before actually making the reading to allow the relay junctions in the signal path to reach thermal equilibrium. To ensure accuracy during program execution, the system covers must be installed. The connections between the DIB and the external references should not be subjected to air currents or thermal gradients.

If the meter reports an error during the external calibration process (perhaps due to a setup error), pmm_xcal_mi displays the contents of the meter's AUXERR and ERRSTB error registers and attempts to clear them. If the registers can be cleared, the operator is prompted to repeat the setup. The program then attempts to calibrate the meter. This is done without restarting pmm_xcal_mi. If the error registers cannot be cleared, then a more significant error exists and pmm_xcal_mi aborts.

Equipment Required

Qty	Model	Description
1	Datron 4910*	10V DC Reference
1	Fluke 742A-10K*	10K Resistor Reference
1	949-785-00	Traceability DIB
4	800-537-02	DIB Interface Cables
1	804-208-00	External Calibration PMM Cable Assembly
* The exact values of the 10V and 10K references must be known before performing the external calibration.		

pmm_xcal_mi Procedure

To achieve proper accuracy during program execution the system covers must be installed. Connections between the DIB and the external references should not be subjected to air currents or thermal gradients.

Refer to Appendix A Device Interface Board (DIB) Interfacing Details for DIB information and for orientation of shield and signal on the connector.

1) Log in to a station window as **checkers**. Checkers may require a password.
2) Secure the DIB (pn 804-785-00) onto the test head. Refer to the Catalyst Test Head Manual (pn 553-700-58) for installation and removal of the DIB.
3) Connect the four cables listed below (pn 800-537-02) from the test head slot containing the PMM channel card and cardlet under test to the DIB external connection bracket (DECB). The four DIB interface cables are connected as follows:
   - Slot x, channel A to DECB-A
   - Slot x, channel B to DECB-B
   - Slot x, channel C to DECB-C
   - Slot x, channel D to DECB-D
     where x denotes the PMM channel card slot number.
4) Connect the four BNCs on the PMM external calibration cable assembly (pn 804-208-00) to the coaxial connectors on the DECB as shown below.
   - PMM A HI to A
   - PMM A LO to B
   - PMM B HI to C
   - PMM B LO to D
5) Load the pmm_xcal_mi checker.

6) Set the termination mode under the RUN button to “Continue on error.”

7) Run the checker by typing **run** and pressing <return>. The program displays the following message shown in the figure Checker Display.

   - The program begins by asking the operator for information to be included in the calibration record file it creates. It asks for the operator's name, model name, serial number, last calibration date of the 10V DC reference, model name, serial number, and last calibration date of the 10K resistance reference. See figure Entry Information Menu Display.

```
PMM External Calibration Program

This program is used to externally calibrate the PMM
in the Mixed Signal and Advanced Mixed Signal Test
Systems.


IMPORTANT!!!

Before running this program the system internal
environment must have been stable for FOUR hours. This
means test system power on and ALL covers in place. DO
NOT CONTINUE IF THESE CONDITIONS ARE NOT MET

Do you wish to continue. (‘y’ or ‘n’) ==>
```

Checker Display

```
Please Enter the following information.

Operator name : Smith

Model name of the DC Voltage Standard : Datron 4910

Serial number of the DC Voltage Standard : a53167

Last Calibration date of the DC Voltage Standard : 1 May, 2002

Model name of the 10K Resistor Standard : Fluke 742A-10K

Serial number of the 10K Resistor Standard : 926331

Last Calibration date of the 10K Resistor Standard : 17 May, 2002
```

Entry Information Menu Display

Making Connections

The program instructs the operator to connect the PMM cables to the DIB.

Checking Jumper Wire Connections

This portion of the program checks to see if the jumper wires are properly connected on the DIB.

1) When the program displays Checking Connections the program first checks the A and B connections. If those are properly connected, the program then checks the C and D jumper wire connections. If the connections are incorrect at either point the user has the opportunity to reconnect the jumper wires.
2) If all the connections are correct, the program displays `The jumper wires are properly connected`. and the user is prompted to enter `c` to continue to the next step.

Measuring Offset in PMM Path

Short all signals at the cable end (not the DIB end) to the shields by connecting all of the banana jacks together.

1) This setup measures offset in the PMM path. When the program displays "Measuring OFFSET in PMM path," make the connections as shown in table PMM Offset Cable Connections using the PMM external calibration cable assembly (pn 804-208-00) provided in the PMM CV Tool Kit.
2) Type `c` to continue the program. Do not disturb the setup while the program is running. The pmm_xcal_mi verifies the connections, waits 5 minutes for all junctions to reach thermal equilibrium, then measures path resistance and voltage offset. These values are used to correct the values of the external standards used later in the calibration.
3) Disconnect all shorted banana jack connections.

PMM Offset Cable Connections

PMM A HI (I1)	SHORT TO	Banana Jack Cable End of PMM B Guard
PMM A LO (I2)		Banana Jack Cable End of PMM A HI
PMM B HI (I3)		Banana Jack Cable End of PMM A LO
PMM B LO (I4)		Banana Jack Cable End of PMM B HI
PMM A Guard		Banana Jack Cable End of PMM B LO
PMM B Guard		Banana Jack Cable End of PMM A Guard

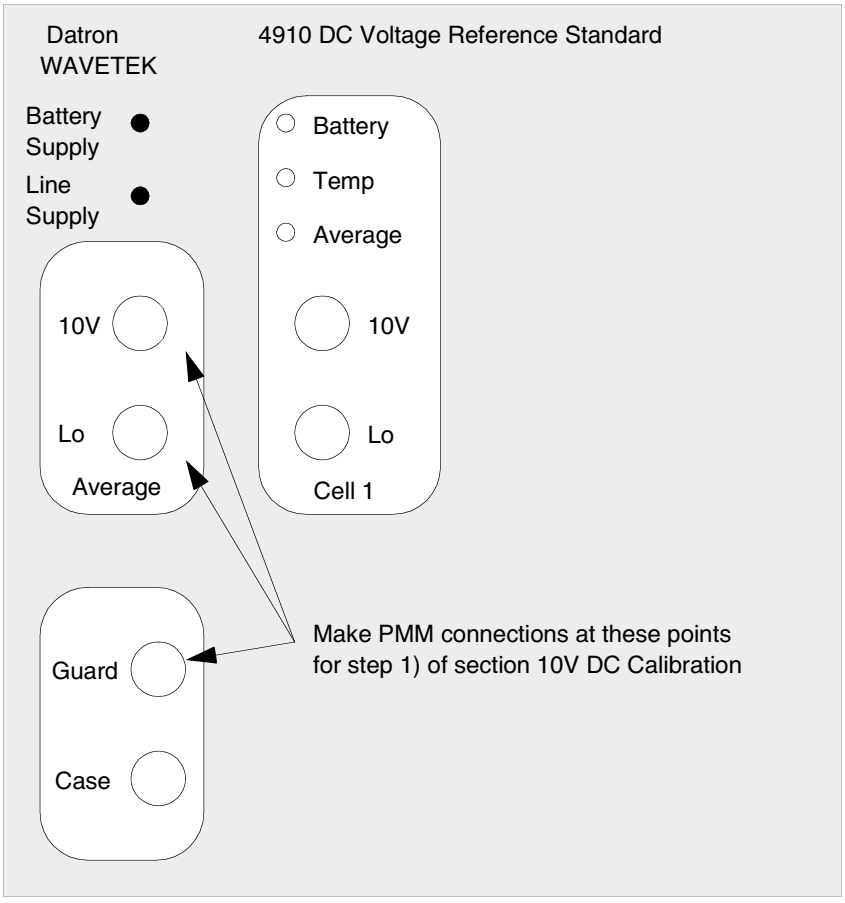
10V DC Calibration

1) When the program displays `10V DC Calibration`, make the following connections between the PMM external calibration (pn 804-208-00) cable assembly and the Datron 4910. Refer to table 10V DC Cable Connections and for the connections. Make the connections using the banana plug end of the cables.

2) Type c to continue the program. Do not disturb the setup while the program is running. The program will query the operator for the value of the 10V DC standard. Type in the value that is displayed on the top of the Datron 4910. Type the value exactly as the program shows. Wait for the program to display the next instruction screen.

10V DC Cable Connections

PMM A HI (I1)	T O	Datron 4910 10V Average
PMM A LO (I2)		Datron 4910 LO Average
PMM A Guard		Datron 4910 Guard/Case



10V DC Calibration Connections on the Voltage Reference Standard

10K Calibration

1) When the program displays 10K Calibration, make the connections as shown in table 10K Calibration Cable Connections between the PMM external calibration cable assembly (pn 804-208-00), provided in the PMM CV Tool Kit, and the Fluke 742A 10 K standard. Make the connections using the banana plug end of the cables.
2) Type `c` to continue the program. Do not disturb the setup while the program is running. After 5 minutes, the program queries the operator for the value of the 10K resistor standard. Type in the value that is displayed on the top of the Fluke 10K resistor standard. Type the value exactly as the program shows.
3) The program displays `Starting PMM 10K Calibration. Time to Completion is 12 Minutes`.
4) Follow the remaining instructions given in the program.
5) When the program is completed, disconnect all external equipment. The process is now complete.

10K Calibration Cable Connections

PMM A HI (I1)	TO	10K Reference High Current
PMM A LO (I2)		10K Reference Low Current
PMM B HI (I3)		10K Reference High Sense
PMM B LO (I4)		10K Reference Low Sense
PMM A Guard		10K Reference Guard (Chassis Ground on Fluke)
PMM B Guard		10K Reference Guard (Chassis Ground on Fluke)

Alternate DC Calibration

As an alternative method of maintaining PMM DC calibration, a customer can choose to remove the HP 3458 meter from the system and calibrate it as an HP 3458 in a qualified calibration lab.

The internal meter temperature at calibration should be within 5°C of the internal meter temperature while operating inside the system. If the internal temperature of the meter changes from its internal temperature at time of calibration by more than 5°C, the PMM accuracy may be affected.

The precision multimeter section of the Catalyst System Specification Manual defines the relevant temperature coefficients to be considered for each specification affected. (See section Example: Implications of Different Calibration and Operation Temperatures.) The internal temperature of the HP 3458 can be determined by using the HP temperature query command `TEMP?` and the internal meter temperature at calibration can be obtained by using CAL? 58, CAL? 59, or CAL? 60. The CAL? query obtains the temperature at calibration of the offset, DCV and resistance references, respectively. (See the HP 3458A Calibration Manual for more details.)

Example: Implications of Different Calibration and Operation Temperatures

Suppose that the temperature of the HP 3458 at calibration is 35.5°C and its temperature while operating inside the system is 43.5°C. The difference between the two temperatures is 8°C, clearly in excess of the 5°C limit. What is the effect on the DCv accuracy of the PMM?

The net effect of the temperature difference can be determined by the following formula:

New_Spec = Old_Spec + (|Txcal -Toper| - 5) * Temp_Coeff

where

New_Spec = New specification due to the difference in temperatures.
Old_Spec = Original specification for operation within 5°C of calibration.
Txcal = Internal temperature of the meter during external calibration.
Toper = Internal temperature of the meter while inside the system.
Temp_Coeff = Temperature coefficient as given in the Specifications Manual for operation outside the 5°C limit.

In the case of DCV accuracy, the 1-year specification on the 1V range is:

DCV Accuracy = 8 ppm of reading + 9 ppm of range

Consultation of the Advanced Mixed Signal Test System Specifications Manual (pn 553-403-56) indicates that the temperature coefficients are 0.15 PMM of reading and 0.1 ppm of range for this temperature difference. From the preceding formula, the new specification for DCV accuracy is:

DCV Accuracy = (8 + (|43.5 - 35.5| - 5) * 0.15) ppm of reading +
(9 + (|43.5 - 35.5| - 5) * 0.10) ppm of range

= (8 + (8-5) * 0.15) ppm of reading +
(9 + (8-5) * 0.10) ppm of range

= 8.45 ppm of reading + 9.3 ppm of range

This is just an example of the DCV accuracy specification. Each operation mode (DC volts, resistance, and DC current) has a unique set of temperature coefficients. Refer to the Catalyst System Manual (pn 553-700-63) for more information.

AC Calibration

The pmm_xcal_mi program does not perform an external AC calibration of the PMM. To do an AC calibration of the PMM, the HP 3458 must be removed from the system and calibrated in a qualified calibration lab according to the HP 3458 calibration manual. Since the AC calibration is relatively insensitive to temperature, calibrating the ac portion of the HP 3458 outside of the system will not affect the PMM performance. It is recommended that AC calibration be performed once every 2 years.

Overview

This chapter describes how to execute the processes that produce data for traceability of Catalyst instruments. Before executing the Level 4 process, it is necessary to install the calibration verification software onto the test system.

Level 4 Calibration Verification Software Installation

1) Log in to a command tool or station window as **`checkers`**.
2) Install the calibration verification CD into the CD drive.
3) Change the working directory to the CD as shown below:

   ```
   cd /cdrom/cdrom0
   ```

4) Execute the `install_cv` script by entering the following command

   ```
   ./install_cv
   ```

   This command puts the calibration verification software into a directory called ~/checkers/CV/CAT/X.Y, where X.Y is the released version of current software, such as 6.2, 6.3, and so on. The directory structure is created if one does not already exist under the ~/checkers directory.
5) The Calibration Verification software installation is now complete.

Level 4 Software Program Loading

Perform the steps below when executing any of the level 4 calibration processes:

1) Log in to the station window under test as **`checkers`**.
2) Move to the directory containing the calibration verification software by entering the following command:

   ```
   cd ~/checkers/CV/CAT/X.Y
   ```

   Where X.Y is the released version of current software, such as 5.3, 5.4, and so on.

3) Load a checker program by highlighting the LOAD button. Pull right to view a list of checkers available, and load a checker program by highlighting it. Alternatively, programs can be loaded by entering - **`load`** *`checkername`*`.load` where *checkername* is the name of the checker to load.

Note

All external instruments throughout the calibration process must have the GPIB option installed and will be connected to the system via the IEEE interface.
Do not connect more than 15 devices to any one bus.
Connect one device for every 6 ft (2 meters) of cable used.
Do not use more than 65 ft (20 m) of cable to connect devices to a bus.
At least two-thirds of the devices on the network must be turned on while the network is operating.
Connect the devices on the network in a star configuration.
Do not use loop or parallel configurations.

atms_cat_cv

Equipment Required

Table 2:

Qty	Model/PN	Description
From the pn 803-804-00 Field CAL Tool Kit:		
1	804-785-00	Catalyst Multipurpose PV/CV DIB
From the pn 803-332-00 HSD and ATMS Traceability Tool Kit:		
1	800-473-00	ATMS Path Length Verification Cable

Setup

- Mount the LA785 DIB to the test head interface
- Connect cable pn 807-326-01 from User Clock on the LA785 DIB to I5B on the strain relief bracket
- Connect cable pn 807-322-00 to I5A on the strain relief bracket

Checker Execution

1) Load atms_cat__cv.load.
2) Run the program, following directions.

Description

This procedure measures the path length error of each tester channel with time measurement specifications. Relative path lengths are measured by connecting an internal user clock signal to the TMS directly and also to the calibration cable. The calibration cable provides connections to each tester channel via program direction to the operator. Time measurements are then made between the internal and external connections. The relative path lengths are compared with each other to determine the path length errors of each channel.

LA785 DIB Information

The program guides the operator through the probing of tester channels with time measurement specifications.

Analog Channel Designation

The program specifies the channel's location in the following format:

Nα

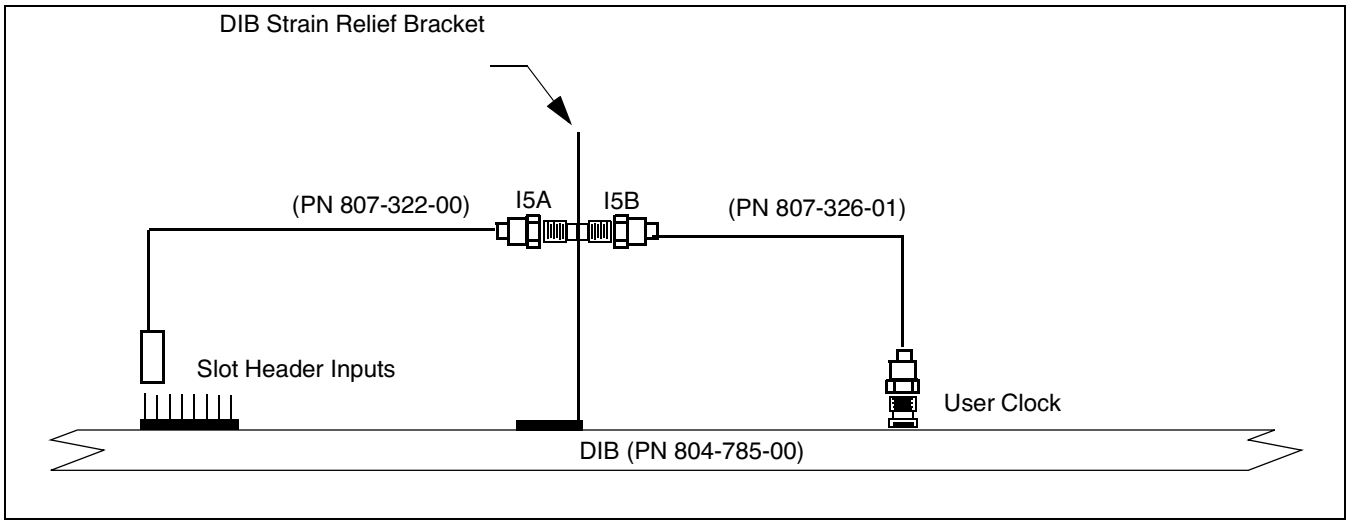
where

- N is the number (2-23) that specifies the channel's test head slot.
- α is an alphabetic character (a, b, c, d) that specifies the channel.

Example:

- See figure 17b is the designation for the header pin in the 17th slot, channel b.
  See the figure table ATMS Calibration Verification Connection Diagram for a connection diagram.

For a detailed description of connecting cables to the two-pin headers, see Appendix A Device Interface Board (DIB) Interfacing Details.



ATMS Calibration Verification Connection Diagram

cat_lfac_cv

This procedure describes the field traceability process (cat_lfac_cv) for the low frequency AC instruments (LFAC): LFAC Source (LFACSrc), and LFAC Digitizer (LFACDig).

The cat_lfac_cv process is menu driven. The user is prompted for all fixture connections, instrument connections, and test selection choices.

Specifications traced are:

- AC amplitude accuracy
- Linearity
- DC offset

Equipment Required

Table 3:

Qty	Model/PN	Description
1	803-808-00	Catalyst PLF/LFAC Tool Kit

External Equipment Required

HP 3458A multimeter with GPIB option (Address = 10)

Runtime Summary

Total run time for one LFACSrc and LFACDig pair is approximately 21 minutes.

Table 4:

Test Name	Run Time
AC Amplitude Accuracy	12 minutes
Linearity	7 minutes
DC Offset	2 minute

Checker Execution

Use the procedure to execute the Catalyst LFAC traceability process:

1) Load cat_lfac_cv into the station under test by entering the following command:

```
load cat_lfac_cv.load
```

2) Run the program and follow all instructions and user prompts displayed.

This series of instructions and prompts appears in the station window:

The following message appears only for as long as the program takes to set up the array processor.

```
Starting LFAC Calibration Verification Process...
```

The program then prompts the user to load the DIB assembly and make all external instrument setup connections.

3) Load the LA723 DIB assembly on the test head.
4) Connect the HP 3458A multimeter to ac power.
5) Connect the HP 3458A multimeter to the system GPIB port with a GPIB cable. (Make sure the HP 3458A GPIB address is set to 10.)
6) Connect the HP 3458A meter input (2 wire) HI and LO to the LA723 BNC jack labeled "BNC1 EXT MTR" using the BNC-to-BNC cable and the BNC-to-BANANA adapter. Refer to the figures LFAC Cable Connections and Catalyst LFACCV Calibration Verification Connections (Not to Scale).

   Press <Return> when ready to go to the next screen.
7) The program then prompts for a serial number of the external meter. Enter the serial number of the HP 3458A meter and press <Return>.
8) The program then prompts for the calibration due date of the HP 3458A meter. Enter the calibration due date of the meter and press <Return>.
9) If the system has more than one set of LFAC instrumentation, the user is prompted to choose one of each to be used during the CV process. The test head slot location of the channel card for the instrument is listed in brackets after each choice. For example:

```
Choose LFAC Source in TH Slot [] to test:
<1> [3]
<2> [20]
ENTER OPTION and <return>:

Choose LFAC Digitizer in TH Slot [] to test:
<1> [3]
<2> [20]
ENTER OPTION and <return>:
```

Note

If only one instrument is in the system, a choice is not offered; the program goes directly to the connection prompts.

10) A prompt is displayed, with specific test head slot connector labels, for connection of the PLFCV DIB port-slot jumper connections (pn 800-487-00). For example, if the LFAC channel card is in slot 3 of the test head, the following prompt appears:

Connect the LFACSRC in test head slot 3 to J10 on the DIB.

Using cable pn 800-487-00, connect pin 1 of J10 to pin 1 of SL3.

Pin 1 on cable pn 800-487-00 is identified by the white marking.

Pin 1 on the J10 and SL3 connectors is always the pin closest to the stenciling on the DIB.

Press <RETURN> when ready.

CONNECT the LFACDIG IN TEST HEAD SLOT 3 to J12 ON the DIB.

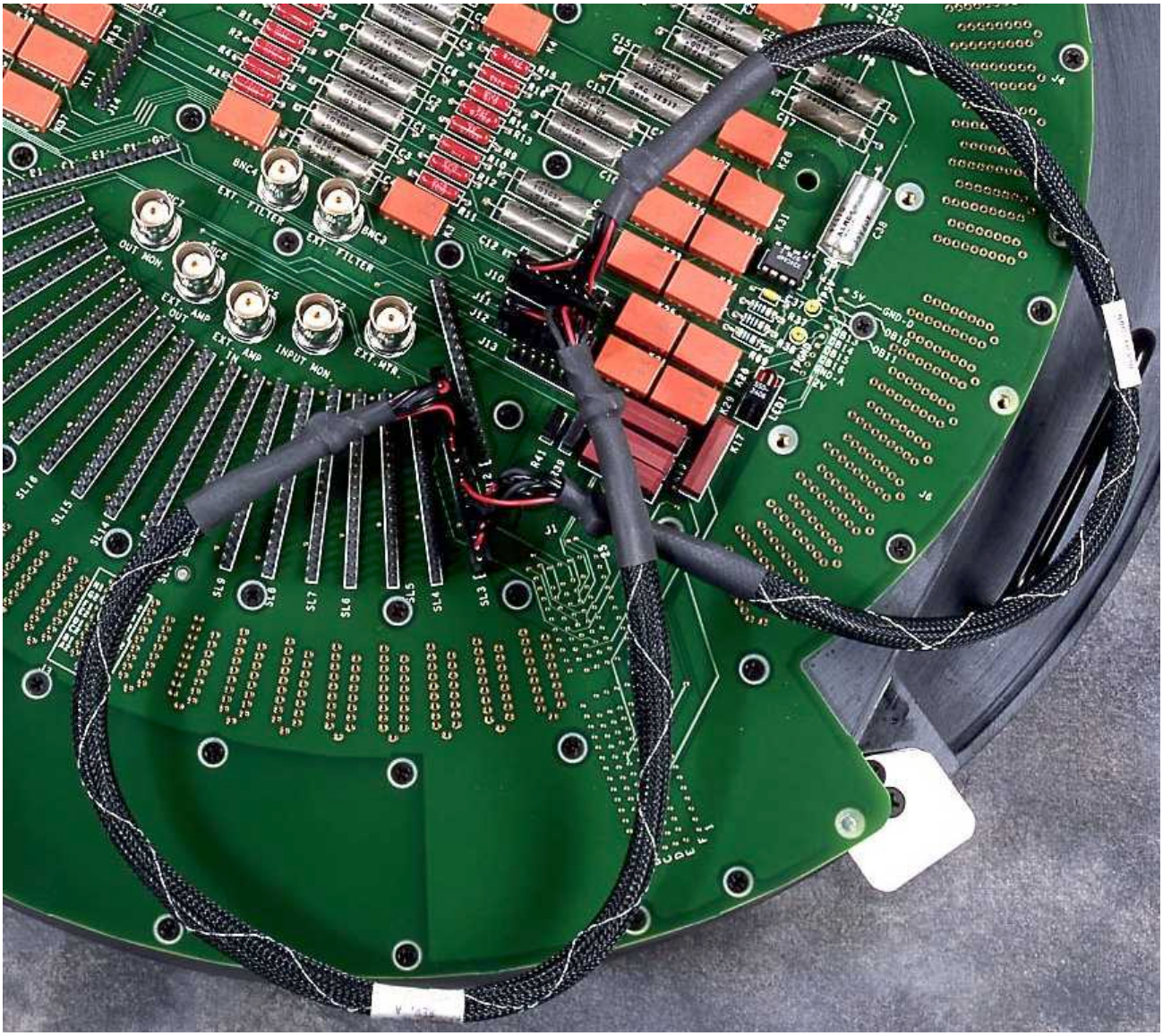
Using cable pn 800-487-00, connect pin 1 of J12 to pin 10 of SL3.

Note that you are connecting to pin 10 of SL3, not pin 1.

Pin 1 on cable pn 800-487-00 is identified by the white marking.

Pin 1 on the J12 and SL3 connectors is always the pin closest to the stenciling on the DIB.

Press <RETURN> when ready.



LFAC Cable Connections

11) After connections are made, the Test Selection menu appears. The user must first make selection(s) of the tests to be run, and then run the tests previously selected. Selected tests have a Y in the Run Test column on the menu.

Normal choices are <A> to select all tests, followed by <C> to execute them. Individual tests can be selected with <number> and <return>. <C> with no tests selected causes the program to exit.

For example, here is the test selection menu as it initially appears:

TEST SELECTION MENU

Testing LFAC DCC TH SLOT:3

	Run Test	Test Name	SRC	DIG
<1>	N	Amplitude Accuracy	Y	Y
<2>	N	DC Linearity	Y	Y
<3>	N	DC Offset	Y	Y
<A>		Select All Tests		
<B>		Select No Tests		
<C>		Run SELECTED Tests or EXIT		

Enter a number to toggle between on and off on a given test. (Run Test=N or Y).
Enter a letter to toggle between all on or off for all tests. (All run test=N or Y).
Selection <C> runs selected tests (Run Test=Y), or exits (All Test=N).
Enter a number or letter and press <return>:

After selecting <A> and pressing <return> the Test Selection menu appears as follows:

TEST SELECTION MENU

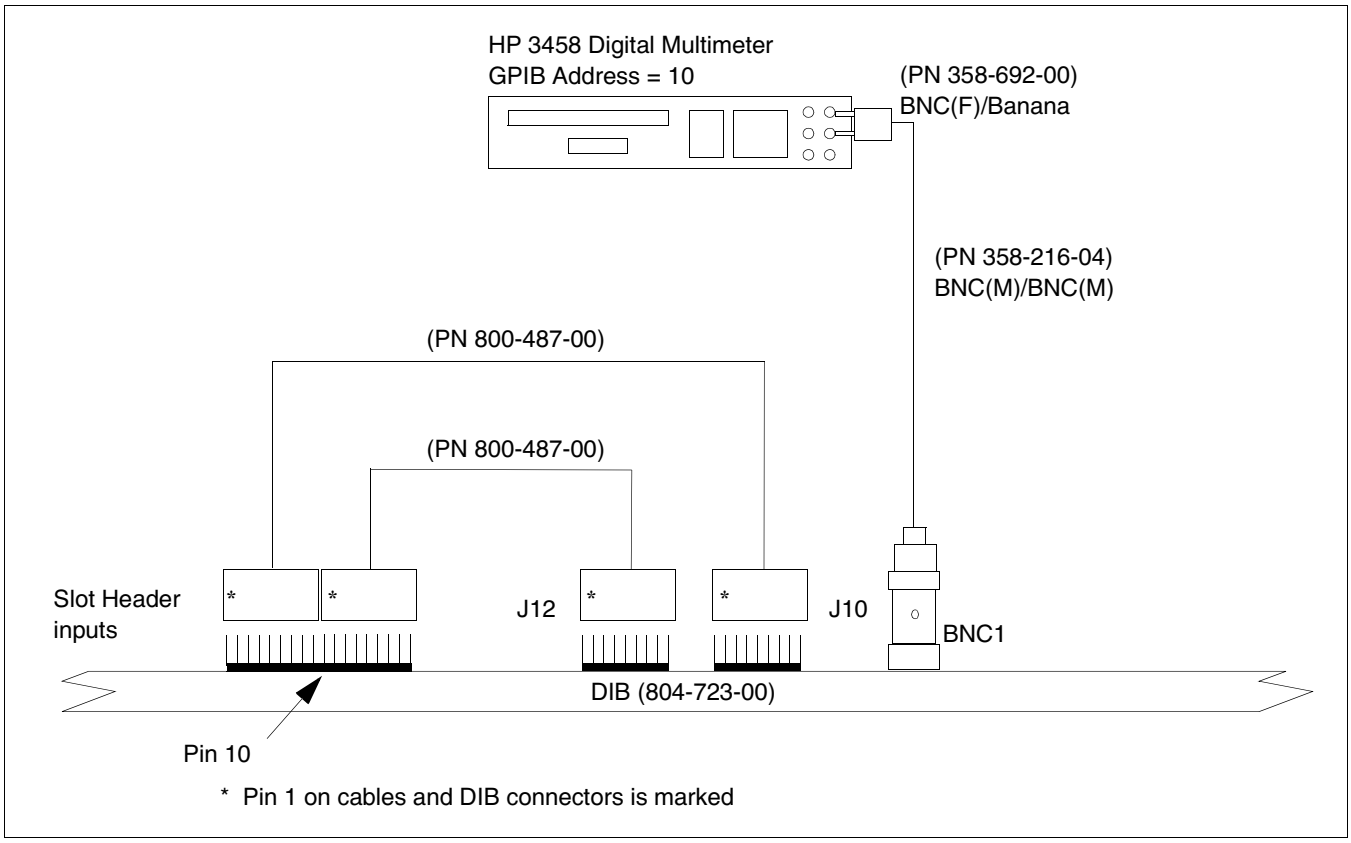
Testing LFAC DCC TH SLOT:3

	Run Test	Test Name	SRC	DIG
<1>	Y	Amplitude Accuracy	Y	Y
<2>	Y	DC Linearity	Y	Y
<3>	Y	DC Offset	Y	Y
<A>		Select All Tests		
<B>		Select No Tests		
<C>		Run SELECTED Tests or EXIT		

Enter a number to toggle between on and off on a given test. (Run Test=N or Y).
Enter a letter to toggle between all on or off for all tests. (All run test=N or Y).
Selection <C> runs selected tests (Run Test=Y), or exits (All Test=N).
Enter a number or letter and press <return>:

12) After <C> is selected to run tests, a message is displayed as the first test begins. For example:
`Running AC Amplitude Accuracy`

13) All selected tests are run and results are put into the BIN at the end of program execution.



Catalyst LFACCV Calibration Verification Connections (Not to Scale)

cat_plf_cv

This procedure describes the field traceability process (cat_plf_cv) for the Catalyst precision low frequency (PLF) instruments: PLF source (PLFSrc) and PLF digitizer (PLFDig).

The cat_plf_cv process is menu driven. The user is prompted for all fixture connections, instrument connections, and test selection choices.

Specifications traced are:

- DC offset
- Linearity
- DC offset drift
- AC amplitude accuracy

Equipment Required

Table 5:

Qty	Model/PN	Description
1	803-808-00	Catalyst PLF/LFAC Tool Kit

External Equipment Required

HP 3458A Multimeter with GPIB option (Address = 10)

Run Time Summary

Total run time for the PLFSrc and PLFDig pair is approximately 26 minutes.

Table 6:

Test Name	Run Time
AC Amplitude Accuracy	12 minutes
Linearity	7 minutes
DC Offset Drift	6 minutes
DC Offset	1 minute

Checker Execution

Use this procedure to execute the Catalyst PLF traceability process.

1) Load cat_plf_cv into the station under test by entering the following command:

```
load cat_plf_cv.load
```

2) Run the program and follow all instructions and user prompts displayed.

This series of instructions and prompts appears in the station window only for as long as the program takes to set up the array processor:

```
Starting PLF Calibration Verification Process...
```

The program then prompts the user to load the DIB assembly and make all external instrument setup connections.

3) Load the LA723 DIB assembly (pn 808-723-00) on the test head.
4) Connect the HP 3458A meter to AC power.
5) Connect the HP 3458A meter to the system GPIB port with a GPIB cable.

Note

Make sure the HP 3458A GPIB address is set to 10.

6) Connect the HP 3458A meter input (2 wire) HI and LO, to the LA723 BNC jack labeled “BNC1 EXT MTR” using the BNC-to-BNC cable and the BNC-to-BANANA adapter. Refer to figure PLFCV Catalyst Calibration Verification Connections.

   Press <return> to go to the next screen.

7) The program then prompts for a serial number of the external meter. Enter the serial number of the HP 3458A meter and press <return>.

8) The program then prompts for the calibration due date of the HP 3458A meter. Enter the calibration due date of the meter and press <return>.

9) If the system has more than one PLFsrc or PLFdig, the user is prompted to choose one of each to be used during the CV process. The test head slot location of the channel card for the instrument is listed in brackets after each choice. For example:

```
Choose PLF Source in TH Slot [] to test:
<1> [3]
<2> [15]
ENTER OPTION and <return>:

Choose PLF Digitizer in TH Slot [] to test:
<1> [4]
<2> [16]
ENTER OPTION and <return>:
```

Note

If only one instrument is in the system, a choice is offered; the program goes directly to the connection prompts.

10) A prompt is displayed, with specific test head slot connector labels, for connection of the DIB port-slot jumper connections (pn 800-487-00). For example, if the PLFsrc channel card in test head slot 3, the following prompt appears:

    Connect the PLFsrc in test head slot 3 to J10 on the DIB.

    Using cable pn 800-487-00, connect pin 1 of J10 to pin 1 of SL3.

    Pin 1 on cable pn 800-487-00 is identified by the white marking.

    Pin 1 on the J10 and SL3 connectors is always the pin closest to the stenciling on the DIB.

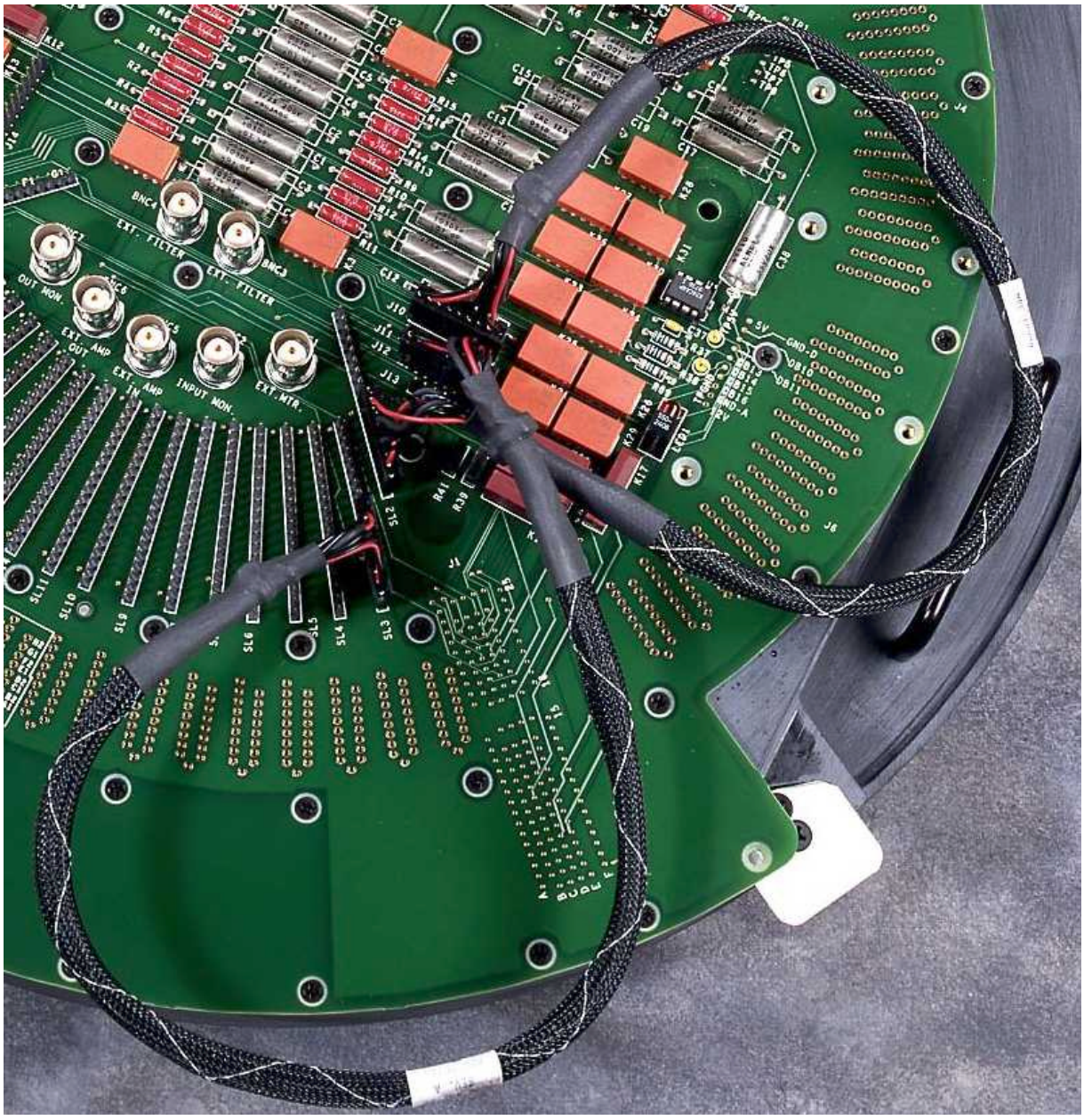
11) If the PLFdig channel card is in test head slot 4, the following prompt appears:

    Connect the PLFdig in test head slot 4 to J12 on the DIB.

    Using cable pn 800-487-00, connect pin 1 of J12 to pin 1 of SL4.

    Pin 1 on cable pn 800-487-00 is identified by the white marking.

    Pin 1 on the J12 and SL4 connectors is always the pin closest to the stenciling on the DIB.



PLF Cable Connections

12) After connections are made, the Test Selection menu appears. The user must first make selection(s) of the tests to be run, and then run the tests previously selected. Selected tests have a Y in the Run Test column on the menu.

Normal choices are <A> to select all tests, followed by <C> to execute them. Individual tests can be selected with <number> and <return>. <C> with no tests selected causes the program to exit.

For example, here is the test selection menu as it initially appears:

TEST SELECTION MENU

Using PLFS TH SLOT: 3PLFD TH SLOT: 4

	Run Test	Test Name	SRC	DIG
<1>	N	Amplitude Accuracy	Y	Y
<2>	N	DC Linearity	Y	Y
<3>	N	DC Offset Drift	Y	Y
<4>	N	DC Offset	Y	Y
<A>		Select All Tests		
<B>		Select No Tests		
<C>		Run SELECTED Tests or EXIT		

Enter a number to toggle between on and off on a given test. (Run Test=N or Y).
Enter a letter to toggle between all on or off for all tests. (All run test=N or Y).
Selection <C> runs selected tests (Run Test=Y), or exits (All Test=N).
Enter a number or letter and press <return>:

After selecting <A> and pressing <return> the test selection menu appears as follows:

TEST SELECTION MENU

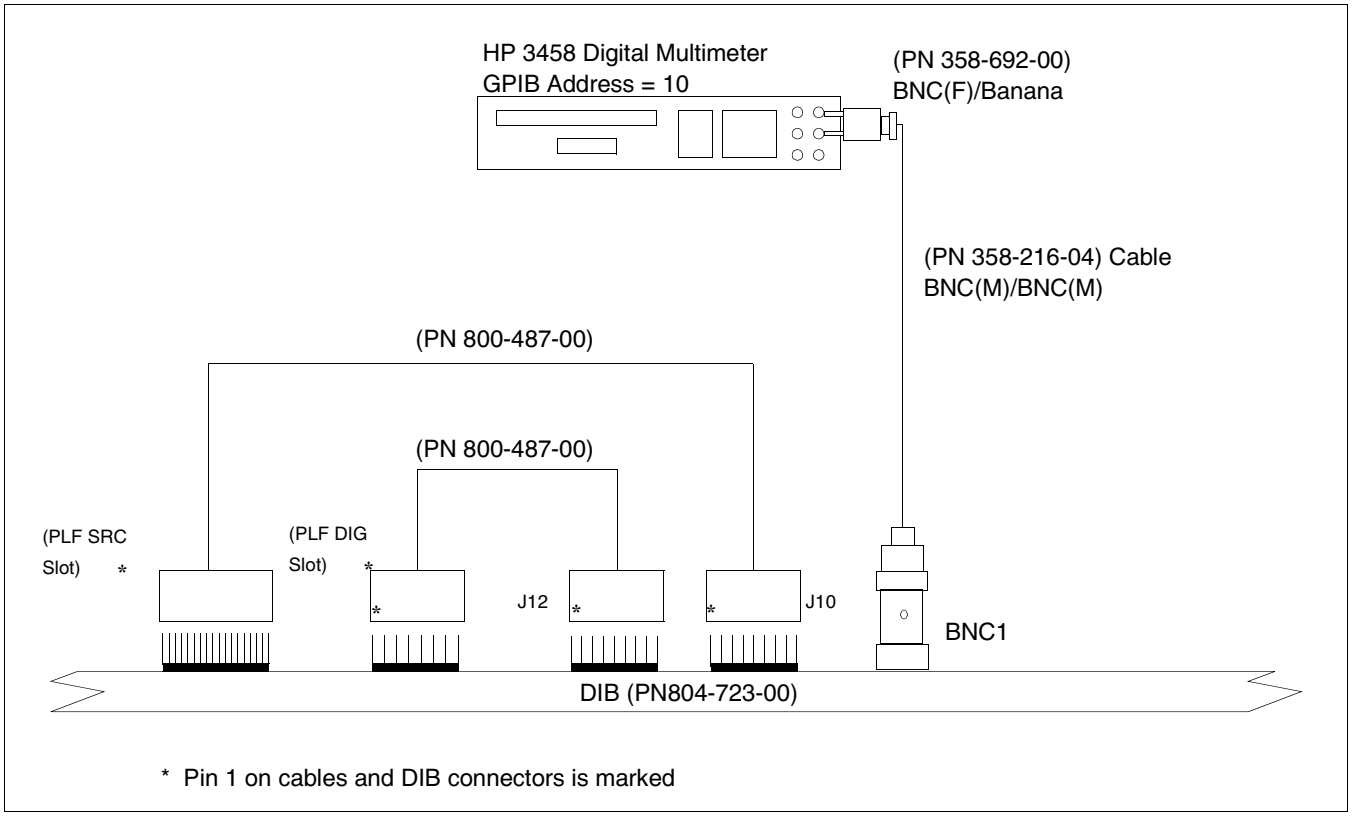
Using PLFS TH SLOT: 3PLFD TH SLOT: 4

	Run Test	Test Name	SRC	DIG
<1>	Y	Amplitude Accuracy	Y	Y
<2>	Y	DC Linearity	Y	Y
<3>	Y	DC Offset Drift	Y	Y
<4>	Y	DC Offset	Y	Y
<A>		Select All Tests		
<B>		Select No Tests		
<C>		Run SELECTED Tests or EXIT		

Enter a number to toggle between on and off on a given test. (Run Test=N or Y).
Enter a letter to toggle between all on or off for all tests. (All run test=N or Y).
Selection <C> runs selected tests (Run Test=Y), or exits (All Test=N).
Enter a number or letter and press <return>:

13) After `<C>` is selected to run tests a message will be displayed as the first test begins. For example: `Running AC Amplitude Accuracy...`

14) All selected tests are run and results are placed in the BIN at the end of program execution.



PLFCV Catalyst Calibration Verification Connections

tjd_cv

Equipment Required

Table 7:

Qty	Model/PN	Description
1	HP 8657	Programmable Signal Generator
From the pn 803-800-00 HSD Catalyst Level III CV Kit:		
1	358-216-04	4ft 50 ohm Coaxial Cable
From the pn 803-804-00 Multipurpose CV DIB Kit:		
1	804-785-00	Multipurpose CV DIB
1	804-322-00	Twisted Pair Cable

Description

This procedure measures both the period and edge jitter of the time jitter digitizer. It also ensures that the device is functionally capable of all ranges of operation. The two time-stamping devices are checked for their reliability over a range of frequencies and under different input front ends.

Setup and Execution

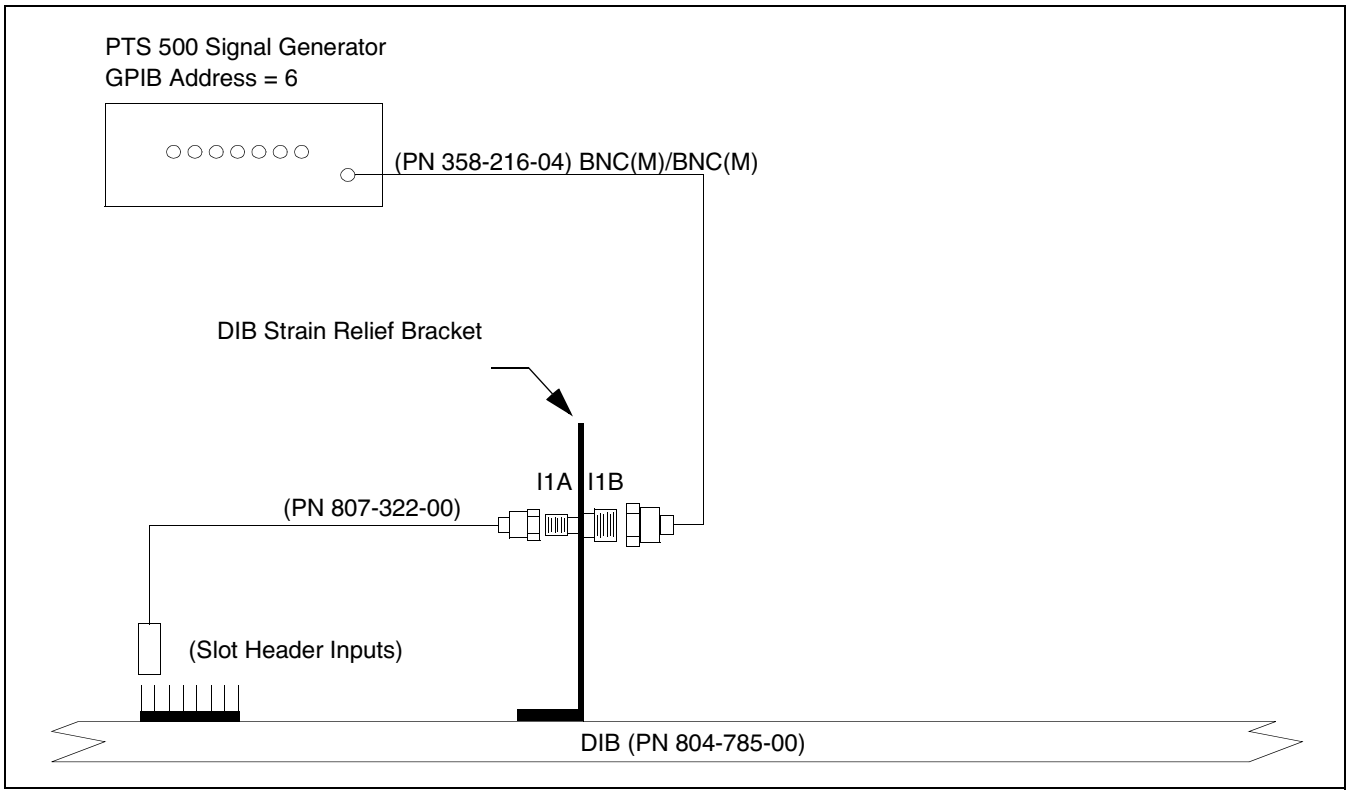
- Load the test program by entering the following command:

  ```
  load thd_cv.load
  ```

- Install the LA785 DIB onto the test head.
- Run the program. Select option 1, Run all tests.
- Connect cable pn 358-216-04 to DIB I1B as instructed by the test program.
- Connect cable pn 807-322-00 to DIB I1A as instructed by the test program.

  During testing, the program instructs the user to connect the other end of cable pn 807-322-00 first to Channel H and then to Channel D.

  For a detailed description of connecting to the DIB two-pin headers, see Appendix A Device Interface Board (DIB) Interfacing Details.
- All tests must pass Bin 1.



TJD Calibration Verification Connections

vhfawg 2500_CV

This process validates the instrument's calibration to level IV requirements. When performed regularly at the prescribed time interval, NIST traceability of the instrument is maintained. All guaranteed ESSD amplitude accuracy and step attenuation specifications are tested.

Run-time for the test process is approximately 15 minutes, excluding test setup.

Program Name

vhfawg2500_cv.load

Equipment Required

Quantity	Model/Part Number	Description
1	803-804-00	Multipurpose DIB Kit
1	803-806-00	Catalyst Level IV Base Kit
1	HP44IX	Power Meter
1	HP8482A	Sensor
1	HP4412A	Sensor
1	HP3458	Multimeter
1	SLP 450	Filter

Note

All SMA connections on the DIB (AD949) need to be torqued to 8 in-lb.

Checker Test Setup

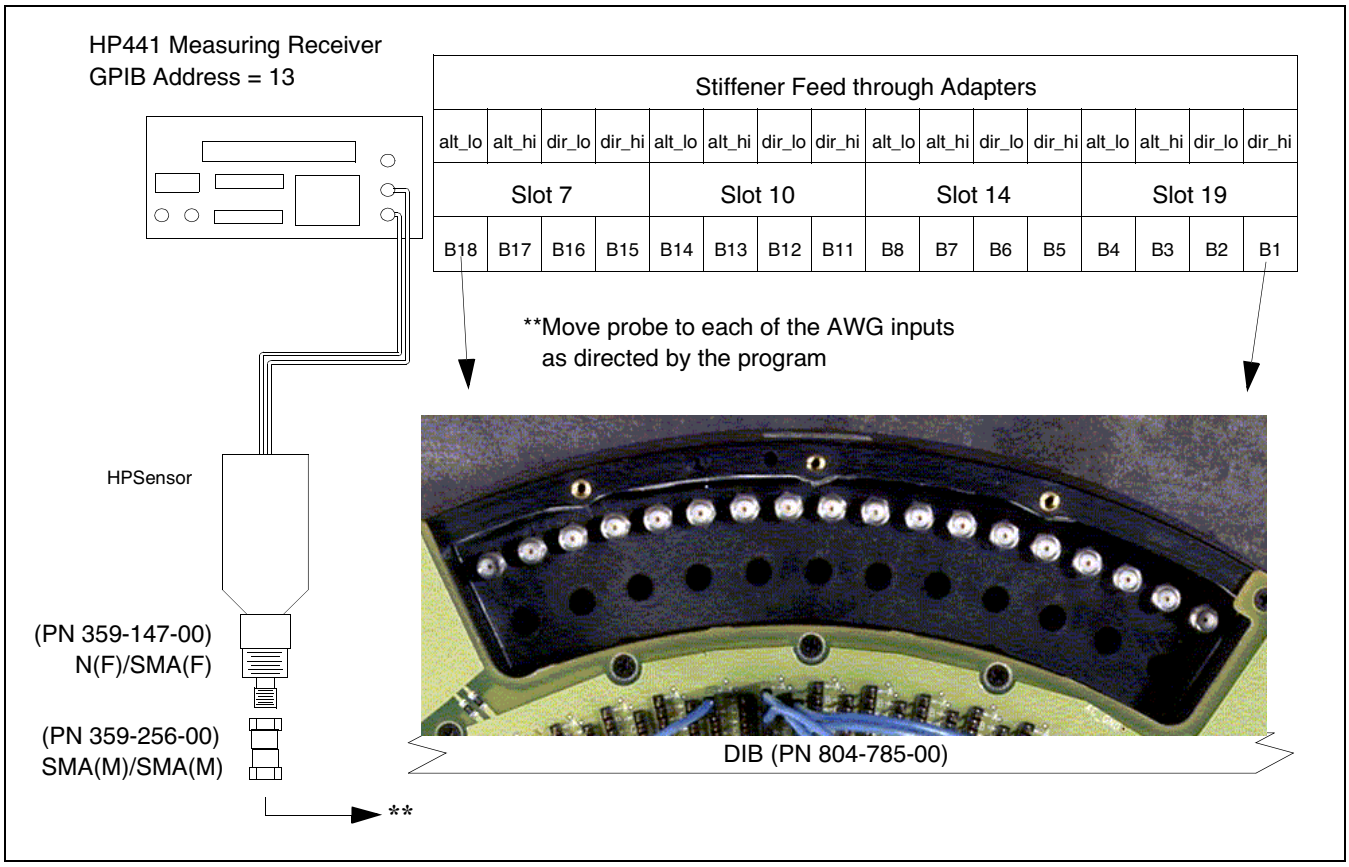
The following setup for the test process is also presented at run-time via the test station window when the program is run.

1) Install the CV DIB onto the test head.
2) The GPIB addresses for the external equipment must be set as follows:
   `Hp441X:13`
   `Hp3458:10`
3) Follow the on-screen instructions for test setup connections for each sequencers.

Checker Test Execution

1) Load and run the VHFAWG2500 CV program. The load file name is *vhfawg2500_cv.load*.
2) Follow the program instructions for instrument traceability and connecting the test setup, as described in the above section.
3) The main menu has two options:
   - Run Absolute Amplitude Tests
   - Run Step Attenuation Tests

   Select and run each test one at a time.
4) Repeat steps three for each instrument in the system.


HP441 Measuring Receiver
GPIB Address = 13
Stiffener Feed through Adapters
alt_lo alt_hi dir_lo dir_hi alt_lo alt_hi dir_lo dir_hi alt_lo alt_hi dir_lo dir_hi alt_lo alt_hi dir_lo dir_hi
Slot 7
Slot 10
Slot 14
Slot 19
B18 B17 B16 B15 B14 B13 B12 B11 B8 B7 B6 B5 B4 B3 B2 B1
**Move probe to each of the AWG inputs as directed by the program
HPSensor
(PN 359-147-00)
N(F)/SMA(F)
(PN 359-256-00)
SMA(M)/SMA(M)
**
DIB (PN 804-785-00)

VHFAWG2500 Calibration Verification Connections

vhfawg 1200 cv

This process validates the instrument's calibration to Level IV requirements. When performed regularly at the prescribed time interval, NIST traceability of the instrument is maintained.

All guaranteed ESSD absolute amplitude and step attenuation specifications are tested.

Runtime for the test process is approximately 15 minutes, excluding test setup.

Program Name

vhfawg1200_catalyst_cv.load

Equipment Required

Table 8:

Qty	Model/PN	Description
1	HP 8902A	Measuring Receiver
1	HP 11722A	Power Sensor
1	803-804-00	Kit, Multipurpose DIB
1	803-806-00	Kit, Catalyst Level IV Base

Checker Test Setup

The following setup for the test process is also presented at runtime via the test station window when the program is run.

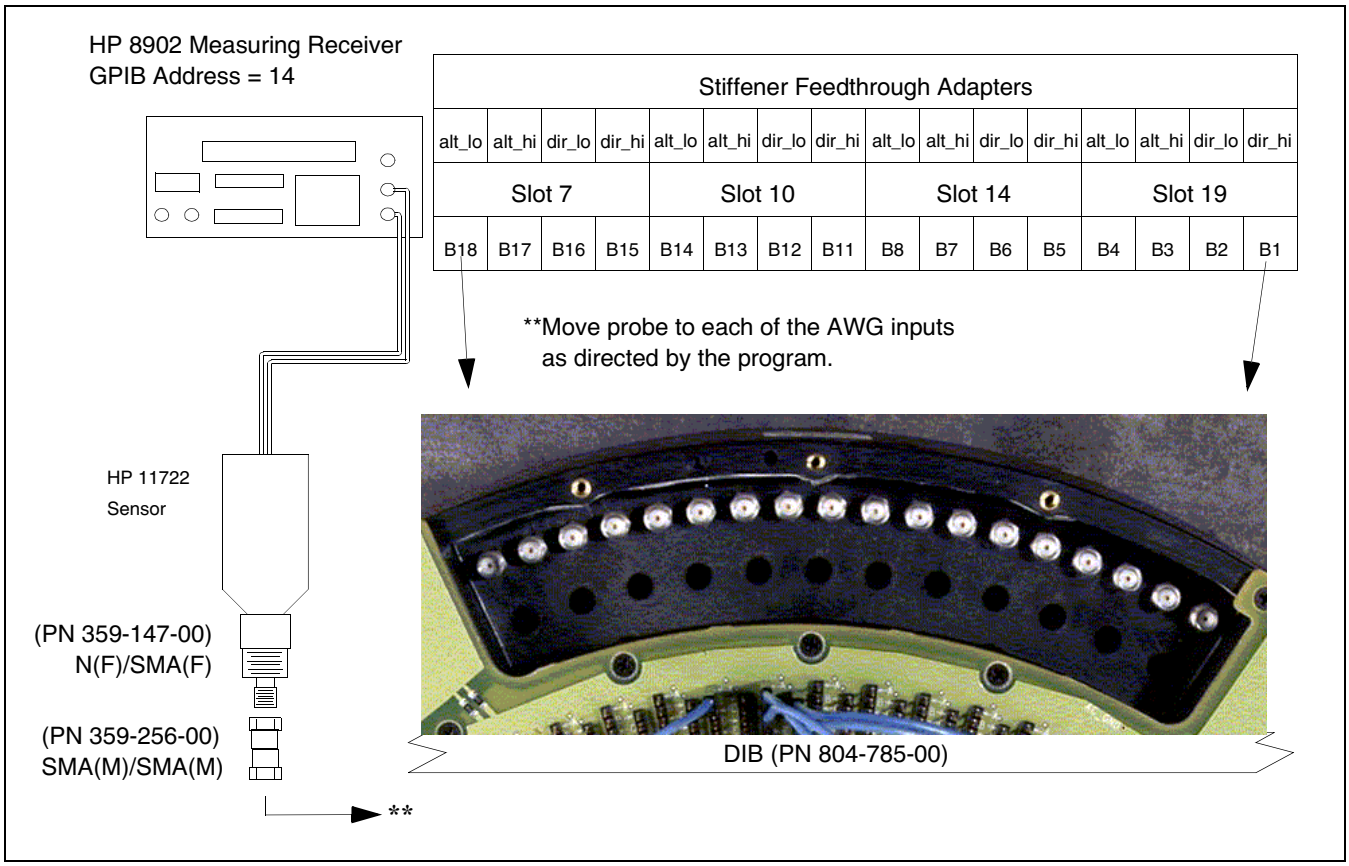
1) Install the CV DIB onto the test head.
2) Connect the HP 11722A power sensor to the HP 8902's RF Power connector for calibration.
3) The GPIB addresses for the external equipment must be set as follows:

```
HP8902A: 14
```

4) Follow the on-screen instructions for test setup connections for each sequencer.

Checker Test Execution

1) Load and run the VHFAWG1200 CV program. The load file name is vhfawg1200_catalyst_cv.load.
2) Follow the program instructions for instrument traceability and connecting the test setup, as described in section Checker Test Setup.
3) The main menu has two options.
   - Select option 1, Run All Tests, to perform one full CV test set on one instrument. Runtime for this automated test process is approximately 15 minutes. A datalog is automatically created.
   - Select option 2, Options Menu, for a list of program options.
4) The Options menu includes the following features:
   - Run Specific CV Tests
   - Support and debug information for each sequencer
5) Repeat steps 3 and 4 for each instrument in the system.


HP 8902 Measuring Receiver
GPIB Address = 14
Stiffener Feedthrough Adapters
alt_lo alt_hi dir_lo dir_hi alt_lo alt_hi dir_lo dir_hi alt_lo alt_hi dir_lo dir_hi alt_lo alt_hi dir_lo dir_hi
Slot 7
Slot 10
Slot 14
Slot 19
B18 B17 B16 B15 B14 B13 B12 B11 B8 B7 B6 B5 B4 B3 B2 B1
**Move probe to each of the AWG inputs
as directed by the program.
HP 11722
Sensor
(PN 359-147-00)
N(F)/SMA(F)
(PN 359-256-00)
SMA(M)/SMA(M)
**
DIB (PN 804-785-00)

VHFAWG1200 Calibration Verification Connections

vhfawg400 diff cv

This process validates of the instrument's calibration to Level IV requirements. When performed regularly at the prescribed time interval, NIST traceability of the instrument is maintained.

All guaranteed ESSD amplitude accuracy and step attenuation specifications are tested.

Runtime for the test process is approximately 20 minutes, excluding test setup.

Program Name

vhfawg400_diff_cv_catalyst

Equipment Required

Table 9:

Qty	Model/PN	Description
1	HP 8902A	Measuring Receiver
1	HP 11722A	Power Sensor
1	803-369-00	HF AC Traceability Tool Kit
1	804-785-00	Catalyst Multipurpose CV DIB

Checker Test Setup

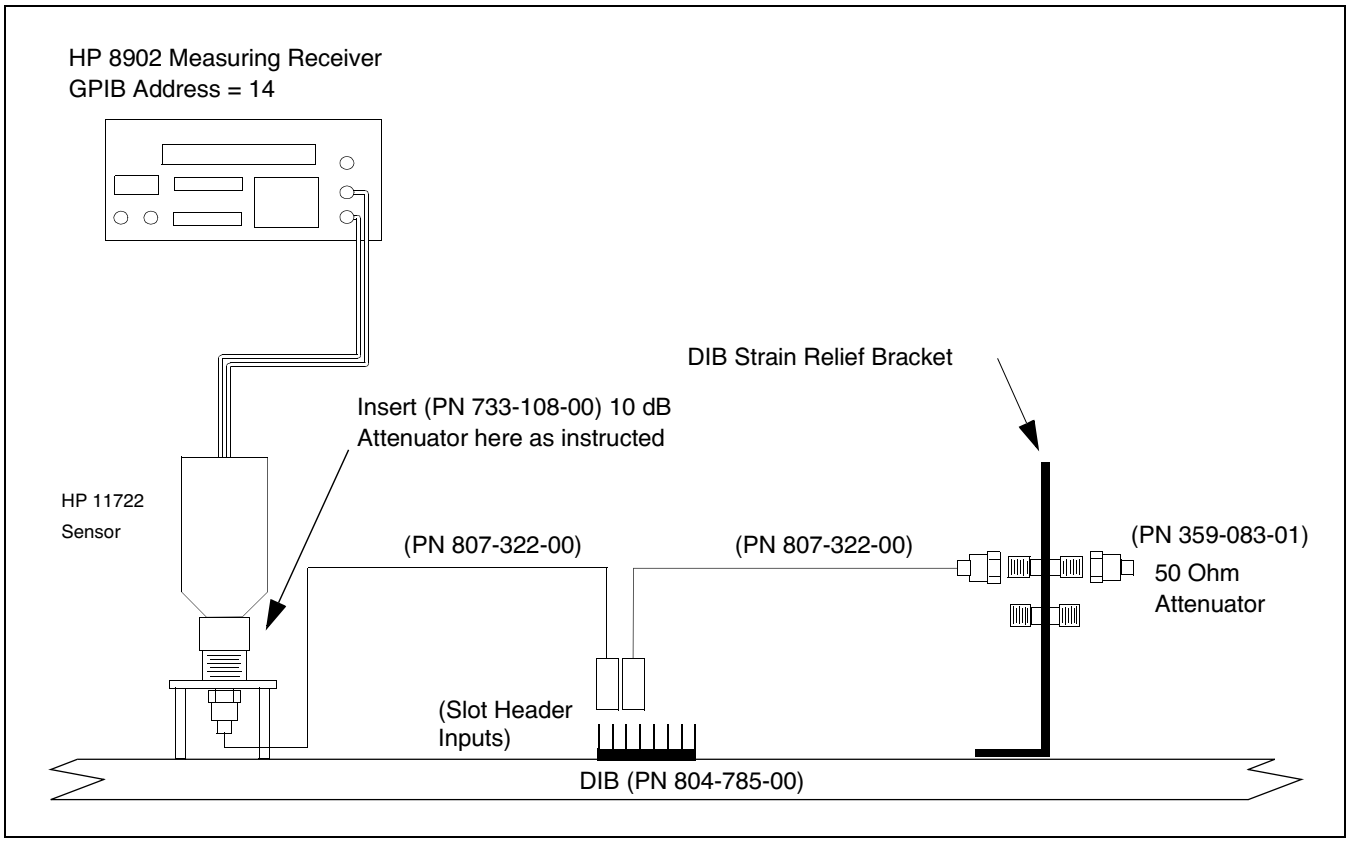
The following setup for the test process is also presented at runtime via the test station window when the program is run.

1) Install the CV DIB (pn 804-785-00) onto the test head.
2) Connect the HP 11722A Power Sensor to the HP 8902's RF Power connector for calibration. After calibration, the sensor is connected to the DIB's N-type adapter.
3) Connect an SMA-to-2-pin cable (pn 807-322-00) to the SMA side of the N-connector.
4) The 2-pin receptacle end of the cable then should be connected to channel A. Refer to the software screen output for further instruction.
5) Connect the 2-pin receptacle end of another SMA-to-2-pin cable with channel B.
6) Connect the SMA end to I6A on the strain relief bracket.
7) Connect the 50 Ω terminator (pn 359-083-00) to I6B of the bracket.
8) For step attenuation, the 10 dB attenuator (pn 359-149-00) should be connected to the N-connector, and the HP 11722A should be connected to the pad. Refer to the software screen output for further instruction.
9) The GPIB address for the external HP 8902 must be set as follows:

```
HP8902A:   14
```

Checker Test Execution

1) Load and run the VHFAWG400 DIFF CV program. The load file name is vhfawg400_diff_cv_catalyst.load.
2) Follow the program instructions for instrument traceability and connecting the test setup, as described in section Checker Test Setup.
3) The Main menu has two options.
   - Select option 1, Run All Tests, to perform one full CV test set on one VHFAWG400 DIFF. Run-time for this automated test process is approximately 20 minutes. A datalog is automatically created.
   - Select option 2, Options Menu, for a list of program options.
4) The Options menu provides the capability to select either Absolute Amplitude or Step Attenuation individually.
5) Repeat steps 3 and 4 for each VHFAWG400 DIFF in the system.



VHFAWG400 DIFF Calibration Verification Connections

hsd_edge_cv

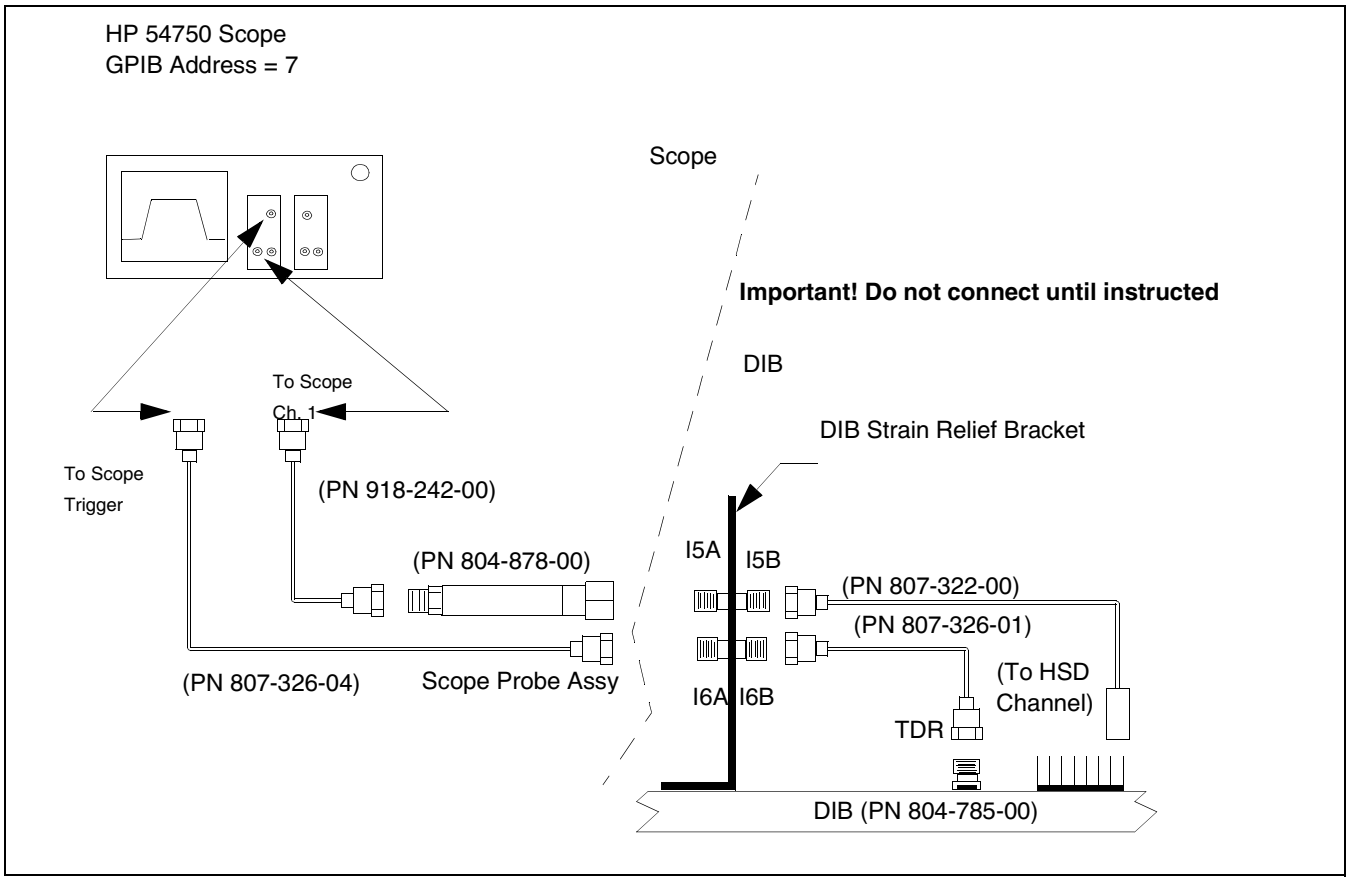
Equipment Required

Table 10:

Qty	Model/PN	Description
1	HP 54750	Digitizing Oscilloscope
From the 803-804-00 Kit, MULTIPURPOSE CV DIB:		
1	804-785-00	DIB Assy.
From the 803-800-00 Kit, Level III LESS PMM:		
1	901-088-00	GPIB Cable (3 Meters length)
From the 803-806-00 Kit, Level IV Base:		
1	807-326-04	Cable, SMA(M)-SMA(M) 4’
1	807-326-01	Cable, SMA(M)-SMA(M) 1’
1	807-322-00	Cable, SMA(M)-2-PIN Header(F) 1’
1	918-242-00	Scope Cable-SMA (male) to SMA (male)
1	804-878-00	Scope Probe Assy.

Checker Execution

1) Load *hsd_edge_cv.load* into Station 1 (or Station 2 if testing test head #2).
2) Lock down the DIB onto the test head under test.
3) Make connections according to the Connection diagram (see figure Catalyst HSD Calibration Verification Connection). Do not make connections to DIB surface until instructed later (after HSD Calibration).



Catalyst HSD Calibration Verification Connection

4) Connect the GPIB cable between the rear of the scope and the GPIB of the system. (Make sure the GPIB address is set to 7.)
5) Run the program.
6) When prompted, enter the scope serial number and scope next calibration date.
7) At the Main menu, press <Return> to run all tests.
8) The program next prompts for the start of edge calibration. Enter your name and then press <Return> to start edge calibration. All calibration sets must pass to continue.

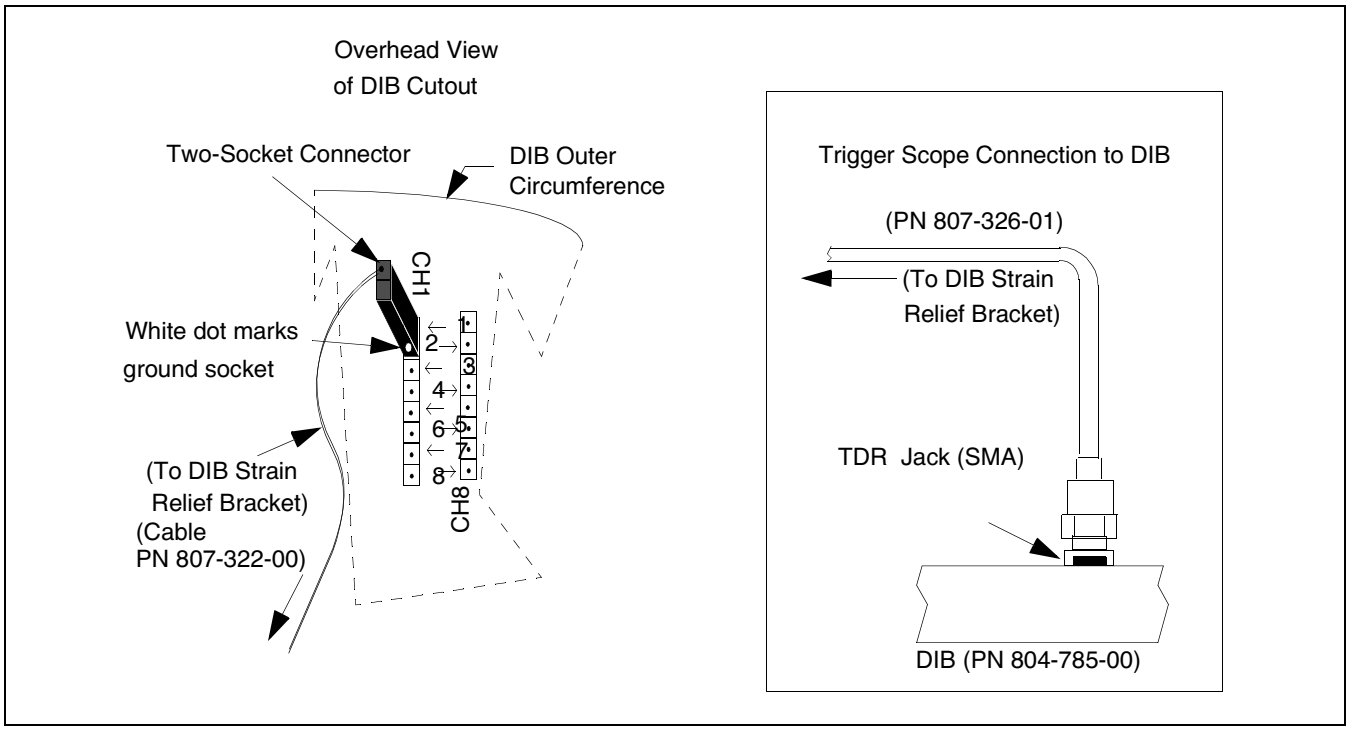
9) When prompted by the program during the reference channel setup, connect the Scope channel to the indicated channel on the DIB (see figure Scope Channel Connection to an HSD DIB Channel).

   Connect the scope trigger by attaching the cable 807-326-01 SMA (M) connector onto the TDR SMA(F) on the DIB surface:

   - Slide the two-socket connector (from pn 807-322-00) over the DIB header pins so that the signal socket (opposite to the white dot) contacts the pin. This pin is pointed to by the silk-screened arrowhead adjacent to the channel number to be tested (channel 1 in the example) on the DIB. The ground socket (marked by the white dot) contacts the adjacent pin to the arrowhead on the DIB.

10) The program then prompts for contact to the channel under test. If the scope is not already connected to that channel, then connect it to that channel. Refer to figure Scope Channel Connection to an HSD DIB Channel. Testing starts after a few-second delay (see note 2).

    When channel testing is completed, the program prompts to move to the next channel. Continue testing until all channels have been tested.



Scope Channel Connection to an HSD DIB Channel

11) After testing of the last channel, the program enters the setup menu. Enter x to exit from the program and to get the final peak-to-peak edge skew of the system.

12) The system must pass each individual channel as well as the peak-to-peak limits in order to complete this process.

13) Remove the connections to the DIB when testing is completed.

Note

If the system fails the peak-to-peak edge skew, the channels that define the range are identified in the summary at the bottom of the datalog. To isolate a faulty board, try swapping CDM or CDTH and note whether the problem follows the swapped board.

Note

If the autodetect feature is disabled, press Enter to begin testing.

Troubleshooting Tip

The first time the digitizing oscilloscope is used to run this process, the scope's frame memory must be Declassified. This is accomplished by pressing the utility button below the display and selecting System Config and Declassify Frame Memory. This procedure is required only the first time the scope is used.

Catalyst 1GHz VHF Digitizer CV

This process validates the instrument's calibration to Level IV requirements. When performed regularly at the prescribed time interval, NIST traceability of the instrument is maintained. All guaranteed ESSD amplitude accuracy and DC accuracy specifications are tested. Run-time for the test process is approximately 30 minutes, excluding test setup.

Program Name

vhfd_cv

Equipment Required

Quantity	Model/Part Number	Description
1	HP11722A	Power Sensor
1	HP8657A	Frequency Synthesizer
1	HP8902A	Measuring Receiver
1	358-216-15	15' BNC-BNC Cable
1	804-785-00 Catalyst 1GHz VHFD CV DIB	
1	807-326-04 4' BNC-SMA cable	
1		

CV Test Setup

The following setup for the test process is also presented at run-time via the test station window when the program is run.

1) Install the Catalyst 1GHz VHFD CV DIB (pn 804-785-00) on to the test head.

2) Manually mate the DIB's RF_HI and RF_LO cables to the appropriate DIB connectors according to the test head slot of the instrument under test. Follow the on-screen instructions.

3) Connect the RF Power output of the HP8657 to the DIB input, I5A, using the 4' BNC-SMA cable (pn 807-326-04).

4) Connect HP11722A power sensor to the HP8902's RF power connector for calibration. After calibration, the program will prompt the user to connect the sensor to the N connector on the DIB.

5) Connect the system 10MHz reference to the TIME BASE INPUT connector of the HP8657 using the 15' cable (pn 358-216-15).

6) The 10MHz reference is generated by the LA703, but can be accessed at the reference output of any PTS in the system, as long as the reference signal daisy chain is not broken. For more information about the location of the LA703, refer to the section on LA703 calibration.

7) The GPIB Addresses for the external equipment must be set as follows:

• HP8902A: 14

• HP8657A: 07

CV Test Execution

1) Load and run the VHFD CV program. The load file name is vhfd_cv.load.

2) Follow the program instructions for instrument traceability and

connecting the test setup, as described in the above section.

3) The Main Menu has two options.

Select option (1), Run All Tests, to perform one full CV test set on one 1GHz VHF Digitizer. Run-time for this test process is approximately 30 minutes. A datalog is automatically created.

Select option (2), Options Menu, for a list of program options. The options menu includes some of the following features.

• Loop CV a User-Defined Number of Times

• Run Specific CV Tests

• Reset the Program for a New Board

Recommend between CV runs to ensure proper test setup.

• Review Test Setup Connections

• Explanation of Test Numbers and Labels

4) Repeat Steps 3 and 4 for each 1GHz VHF Digitizer in the system.

Note

User Power, Stored Data Bits, and Matrix Lines must be operational. The continuity checker can be run to verify their functionality.

VHF Digitizer CV

This process validates the instrument's calibration to Level IV requirements. When performed regularly at the prescribed time interval, NIST traceability of the instrument is maintained.

All guaranteed ESSD amplitude accuracy specifications are tested.

Runtime for the test process is approximately 30 minutes, excluding test setup.

Program Name

vhfd_cv

Equipment Required

Table 11:

Qty	Model/PN	Description
1	HP 8902A	Measuring Receiver
1	HP 11722A	Power Sensor
1	HP 8657A	Frequency Synthesizer
1	807-326-04	4' BNC-SMA cable
1	358-216-15	15' BNC-BNC cable
1	359-164-00	N (plug) - BNC (jack)
1	804-785-00	Catalyst Multipurpose CV DIB

Checker Test Setup

The following setup for the test process is also presented at runtime via the test station window when the program is run:

1) Install the DIB (pn 804-785-00) onto the test head.
2) Manually mate the DIB's RF_HI, RF_LO, HI, and LO cables to the appropriate DIB connectors according to the test head slot of the instrument under test.

   Follow the on-screen instructions for detailed cable connection statements.
3) Connect the RF Power output of the HP 8657 to DIB input I5A, using the N-BNC adapter (pn 359-164-00) and 4 ft. cable (pn 807-326-04).
4) The program prompts the user to connect the HP 11722A power sensor to the HP 8902 RF Power connector for calibration.

   After calibration, the power sensor is connected to the DIB's N-type connector.
5) Connect the system 10 MHz reference to the TIME BASE INPUT connector of the HP 8657 using the 15 ft. cable (pn 358-216-15).

   The 10 MHz reference is generated by the LA703, but can be accessed at the reference output of any PTS in the system, as long as the reference signal daisy chain is not broken. For more information about the location of the LA703, refer to the section LA703 Adjustment Procedure.
6) The GPIB Addresses for the external equipment must be set as follows:
   ```
   HP 8902A: 14
   HP 8657A: 07
   ```

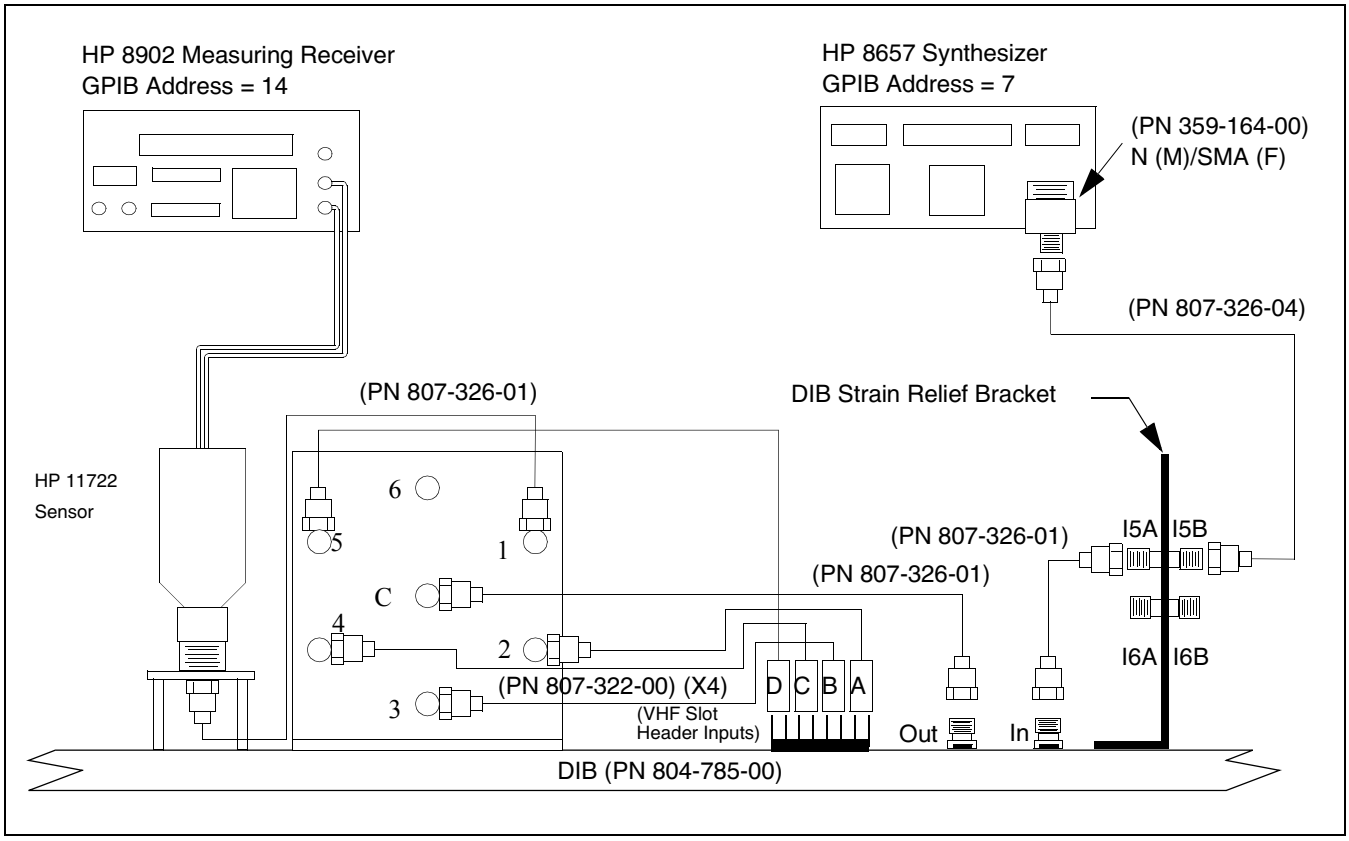
Checker Test Execution

1) Load and run the VHFD CV program. The load file name is vhfd_cv.load.
2) Follow the program instructions for instrument traceability and connecting the test setup, as described in the section Checker Test Setup.
3) The Main menu has two options.
   - Select option 1, Run All Tests, to perform one full CV test set on one VHF Digitizer. Runtime for this automated test process is approximately 30 minutes. A datalog is automatically created.
   - Select option 2, Options Menu, for a list of program options.
4) The Options menu includes the following features:
   - Loop CV a User-Defined Number of Times
   - Run Specific CV Tests
   - Reset the Program for a New Board*
   - Review Test Setup Connections
   - Explanation of Test Numbers and Labels

   *Recommend between CV runs to ensure proper test setup.
5) Repeat steps 3 and 4 for each VHF Digitizer in the system.

Note

User power and stored data bits must be operational.



VHFD Calibration Verification Connections

vhfcw_cv

This process validates the instrument's calibration to Level IV requirements. When performed regularly at the prescribed time interval, NIST traceability of the instrument is maintained.

All guaranteed ESSD amplitude accuracy and step attenuation specifications are tested.

Runtime for the test process is approximately 20 minutes, excluding test setup.

Program Name

beta_vhfcwcv

Equipment Required

Table 12:

Qty	Model/PN	Description
1	HP 8902A	Measuring Receiver
1	HP 11722A	Power Sensor
1	733-108-00	10 dB Attenuator (N)
1	804-785-00	Catalyst Multipurpose CV DIB

Checker Test Setup

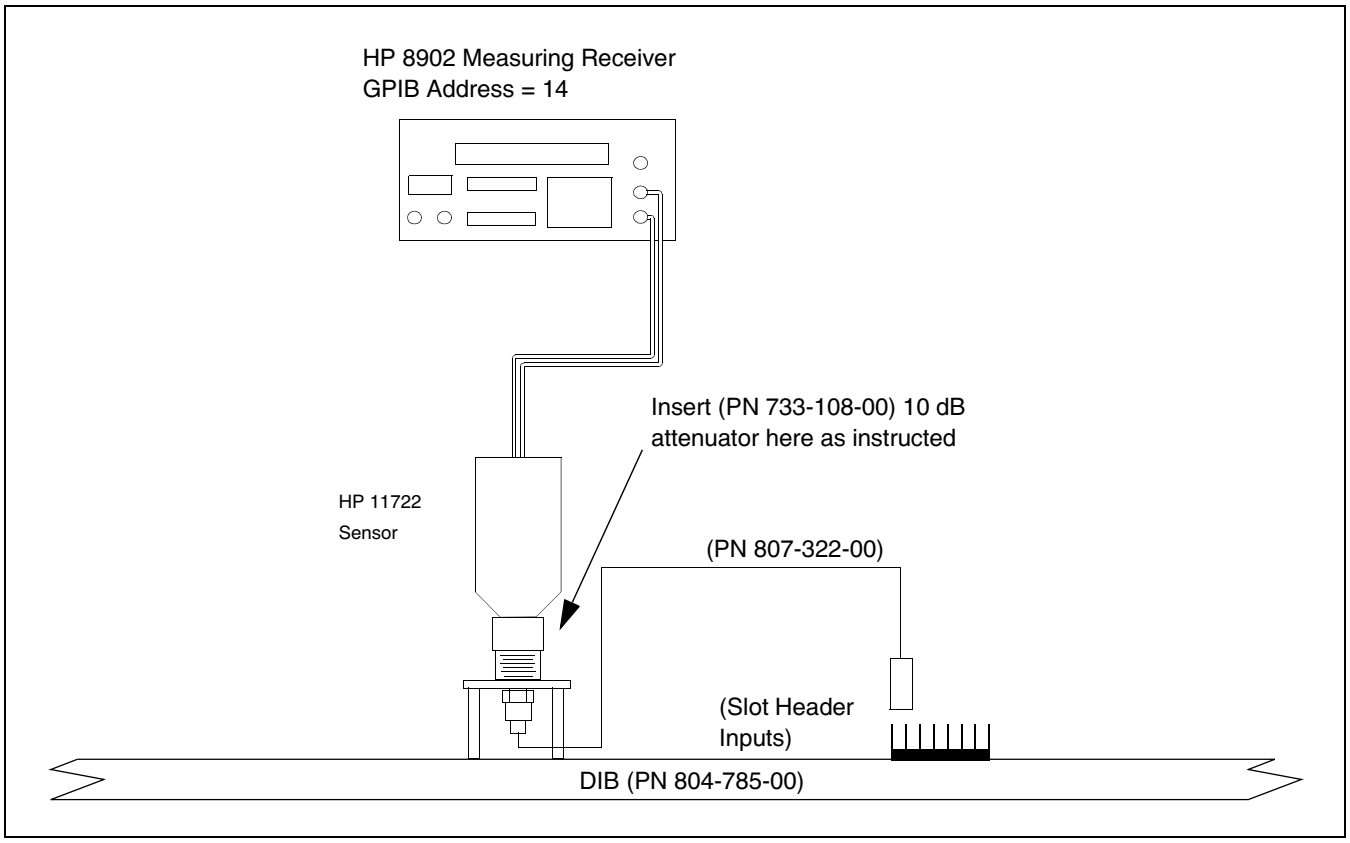
The following setup for the test process is also presented at runtime via the test station window when the program is run.

1) Install the CV DIB (pn 804-785-00) onto the test head.
2) Connect the HP 11722A power sensor to the HP 8902 RF Power connector for calibration. After calibration, the sensor is connected to the DIB's N-type adapter.
3) Connect an SMA-to-2-pin cable (pn 807-322-00) to the SMA side of the N-connector.
4) The 2-pin receptacle end of the cable should then be connected to channel A. Refer to the software screen output for further instructions.
5) For step attenuation, the 10 dB attenuator (pn 733-108-00) should be connected to the N-connector, and the HP 11722A should be connected to the pad.

   Refer to the software screen output for further instructions.
6) Set the GPIB address for the external HP 8902 as follows:
   `HP 8902A: 14`

Checker Test Execution

1) Load and run the VHFCW CV program. The load file name is *beta_vhfcwcv.load.*
2) Follow the program instructions for instrument traceability and connecting the test setup, as described in section Checker Test Setup.
3) The Main Menu has two options.
   - Select option (1), *Run All Tests*, to perform one full CV test set on one VHFAWG400 DIFF. Run-time for this automated test process is approximately 20 minutes. A datalog is automatically created.
   - Select option (2), *Options Menu*, for a list of program options.
4) The Options Menu provides the capability to select either Absolute Amplitude or Step Attenuation individually.
5) Repeat Steps 2 through 4 for each VHFCW in the system.



VHFCW Calibration Verification Connections

uw6000_cv Calibration Procedure

Instrument performance is specified at the test head on the Device Interface Board (DIB). All measurements for the calibration will be made at the DIB. Refer to the figure Layout of the 866-532-00 CV DIBfor DIB connections used with the uw6000_cv program.

Estimated Time Matrix

The different times needed to run the uw6000_cv checker are shown in table Level 4 ETM.

Level 4 ETM

Table 13

Program	Estimated Time
uw6000_cv	5 minutes (source) 42 minutes (quad-port VNA) 84 minutes (octo-port VNA)

Overview

The uw6000_cv checker is a level 4 test. Instrument performance is specified at the test head on the Device Interface Board (DIB). All measurements for the calibration will be made at the DIB. Refer to figure Layout of the 866-532-00 CV DIB for DIB connections used with the uw6000_cv program.

Required Equipment

Required Equipment

Quantity	Model PN	Description
1	HP 83623	Synthesized Sweeper w/GPIB and Opt. 001
1	HP E4418	Power Meter w/GPIB
1	HP E4412A	Power Sensor
1	803-806-00	Kit, Level IV Base
For systems with a Signal Delivery Frame (SDF)		
1	806-126-00	Kit, Catalyst Microwave PV/CV DIB-SDF
For systems with an interim pipe-pan		
1	806-127-00	KIT, Catalyst Microwave PV/CV DIB-INTR

Note

All external instruments throughout the calibration process must have the GPIB option installed and be connected to the system through the IEEE interface. Do not connect more than 15 devices to any one bus. Connect one device for every 6 ft (2 m) of cable used. Do not use more than 65 ft (20 m) of cable to connect devices to the bus. At least two-thirds of the devices on the network must be turned on while the network is operating. Connect the devices on the network in a star configuration. Do not use loop or parallel connections.

GPIB Addresses must be set as follows:
HP 83623:19
HP E4418:13

Runtime Summery

Process Run Time

Test Name	Run Time
Source Level Accuracy	10 mintues / UWSRC CC 12 minutes / UWPORT CC (quad-port) 24 minutes / UWPORT CC (octo-port)
Receive Level Accuracy	30 minutes / UWPORT CC (quad-port) 60 minutes / UWPORT CC (octo-port)

Test Execution

Type `load uw6000_cv.load` and press <RETURN> to load the uw6000_cv.load program.

1) Type `run` and press <RETURN>.

Note

A menu is displayed listing the UW6000 options in the system. The UW6000 Modulated Source Option is indicated by [UWMS] appended to the option name. The Modulated Source Amplitude Accuracy tests are automatically run during this process. This process should be performed on all options.

UW6000 CV Option Selection Menu

```
UW6000 CV: Select an Option to Verify

 No.    Description
-----   -----------------------------------------------
  1     UW6000 VNA - UWPORT Module - Slot 15: SN 0211c50
  2     UW6000 Source - UWSRC Module - Slot 19: SN 024db30
        [UWMS]
  3     UW6000 Source - UWSRC Module - Slot 20: SN 01d8a8d

        Enter a choice or 'X' to Exit (1-3)[1]:
```

Note

This menu shows a system with one UW6000 VNA option, two UW6000 stand-alone source options, and one UW6000 modulated source (behind source slot 19).

2) Enter the number of the option to verify.

Note

The following steps will be displayed only the first time through this process.

3) Attach the 866-532-00 DIB to the test head.

Note

For systems with an interim pipe-pan, substitute the 866-533-00 DIB

4) Set up the HP E4418 power meter for testing by:
   - Plugging the AC power line into an outlet.
   - Connecting a GPIB cable from the system to the meter.
   - Attaching the power sensor and power sensor cable.
   - Setting the GPIB address to 13.
5) Set up the HP 83623 synthesized sweeper for testing by
   - Plugging the AC power line into an outlet.
   - Connecting a GPIB cable from the meter to the sweeper.
   - Attaching the SMA(f) end of the GPIB cable to the RF output.
   - Connecting the system's 10 MHz Ref to 10 MHz Ref Input
   - Setting the GPIB address to 19
6) Enter the serial number of the HP E4418 power meter.
7) Enter the calibration due date of the HP E4418 power meter
8) Enter the serial number of the HP E4412A power sensor.
9) Enter the calibration due date of the HP E4412A power sensor
10) If the HP E4412A power sensor has been zeroed and calibrated, enter Y. Otherwise, enter N and follow the instructions on the screen.

Note

The HP E4412A power sensor must be zeroed and calibrated before the first use, after every hour or when the ambient temperature changes more than 5°F (-15°C).

Note

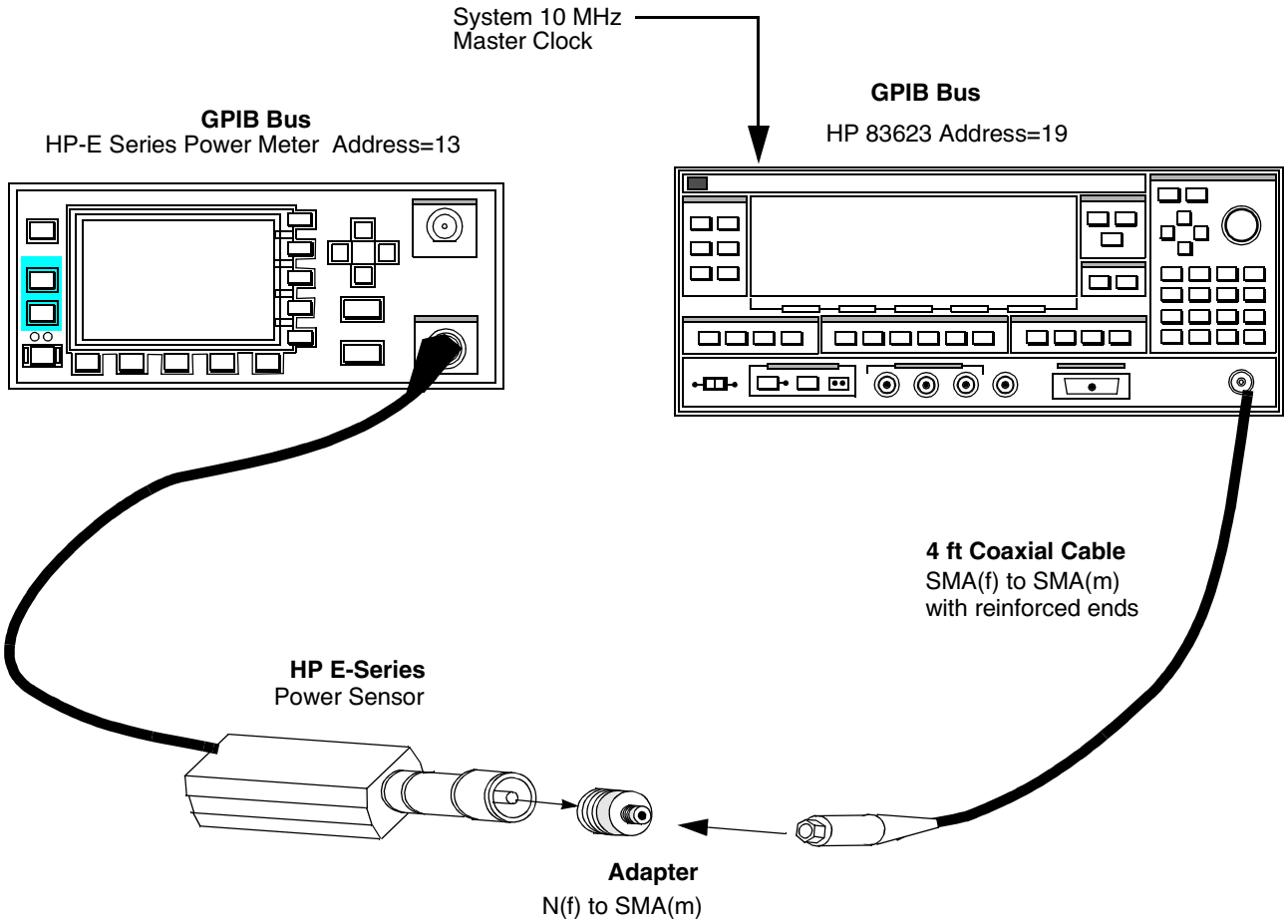
The program will prompt only for the synthesized sweeper information if the UW6000 VNA Option was selected from the menu.

11) Enter the serial number of the HP 83623 synthesized sweeper.

12) Enter the calibration due date of the HP 83623 synthesized sweeper.

13) If the HP 83623 synthesized sweeper has been flattened, enter Y. Otherwise, enter N and follow the instructions on the screen.

See figure Setup for Flattening the Synthesized Sweeper for setup connections.



Setup for Flattening the Synthesized Sweeper

14) If a UW6000 VNA Option was selected, go to section UW6000 VNA Verification.

15) If a UW6000 Source Option was selected, go to section UW6000 Stand-alone Source Verification.

UW6000 VNA Verification

The program will display the UW6000 VNA CV menu as shown in figure UW6000 VNA CV Menu.

1) After performing both options, enter x and return to step 3 of section UW6000 CV Option Selection Menu.

2) Enter the desired option at the prompt.

UW6000 VNA CV Process

No.	Description
1	Source Side
2	Receive Side

Enter a choice or 'X' to Exit (1-2)[1]:

UW6000 VNA CV Menu

3) If you chose the source side option from the menu above, go to section Source Side Process. If you chose the receive side option from the menu, go to section Receive Side Process.

Source Side Process

The program displays a menu listing all valid source channels for the UW6000 VNA selected, as shown in figure Source Side Process Menu. If a modulated source is present, [UWMS] is appended to channels 1 and/or 3, as appropriate.

1) After performing the source side process on all channels, enter x and return to step 2 of section UW6000 VNA Verification.

2) Enter the desired option at the prompt:

SOURCE SIDE PROCESS

No.	Description
1	Channel 1
2	Channel 2
3	Channel 3 [UWMS]
4	Channel 4

Enter a choice or 'X' to Exit (1-2)[1]:

Source Side Process Menu

Note

The menu shown would apply for a quad-port VNA with a modulated source behind the second source.

3) Perform the connection instructions on the screen and press <RETURN>. See figure Source Side Verification Setup.

4) If the test passed, press <RETURN> and return to step 2 of section Source Side Process. If the test does not pass, recheck the connections, press <RETURN>, return to step 2 of section Source Side Process, and repeat the test on this channel.

Note

If a channel fails more than once, you may need to exit and restart the program to rezero and recalibrate the power meter. If the channel continues to fail, you could have a bad UWPORT channel card, UHFSRC channel card, Modulated Source, or FS1000.

Receive Side Process

The program displays the menu shown in figure Receive Side Process. Only channels 1 and 3 require testing.

1) After performing the receive side process on both channels, enter x and return to step 2 of section UW6000 VNA Verification.

2) Enter the desired option at the prompt:

```
RECEIVE SIDE PROCESS

   No.   Description
  ----   -------------
1    Channel 1
2    Channel 3

   Enter a choice or 'X' to Exit (1-2)[1]:
```

Receive Side Process Menu

3) Perform the connection instructions on the screen and press <RETURN> to continue. See figure Receive Side Verification Setup for an illustration.

4) If the test passed, press <RETURN> and go back to step 2.
If the test did not pass, recheck the connections, press <RETURN> and go back to step 2, and repeat the test of the desired channel.

Note

If a channel fails more than once, you may need to exit and restart the program to reflatten the sweeper. If the channel continues to fail, you could have a bad UWPORT channel card or UWMM channel card in the test head.

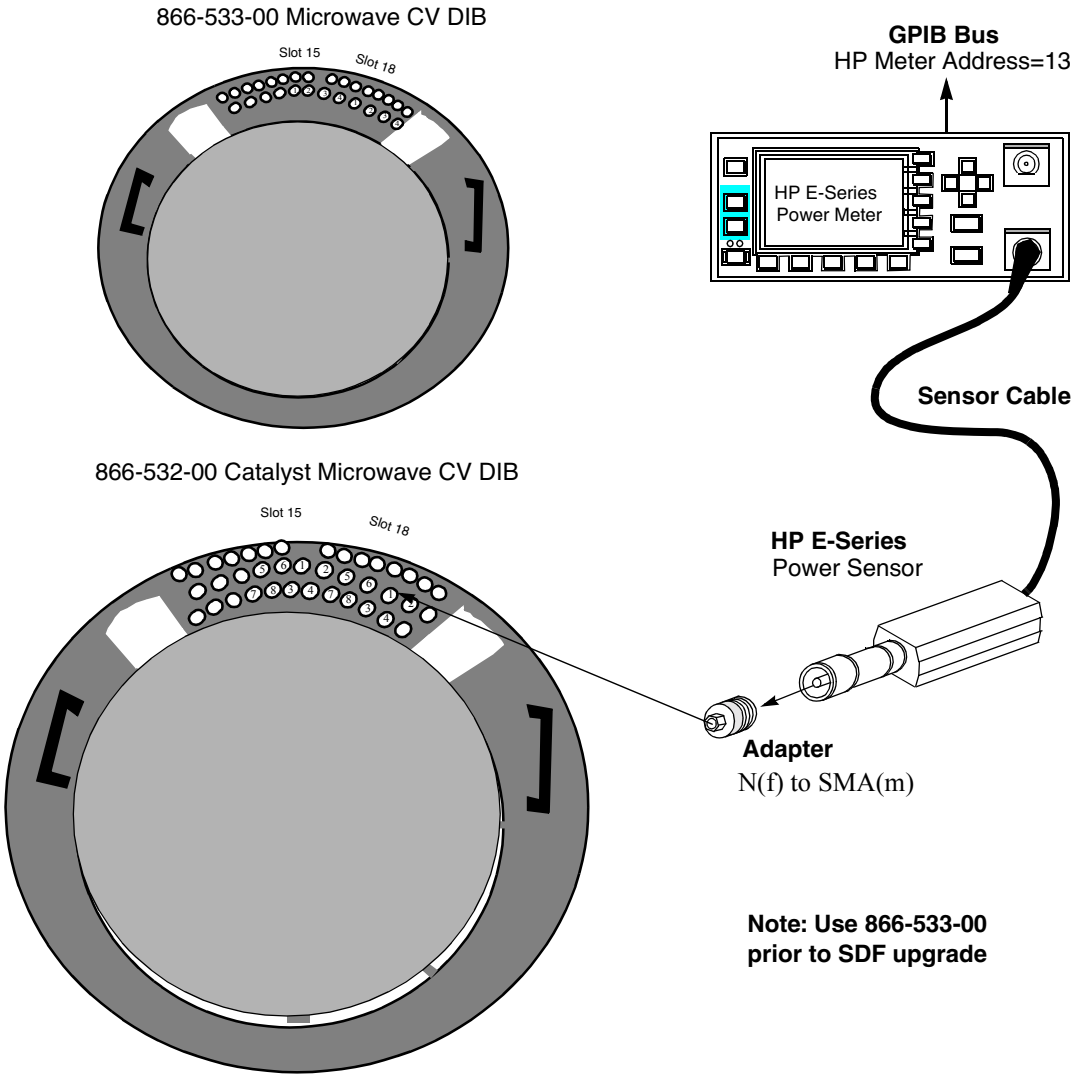
UW6000 Stand-alone Source Verification

Perform the connection instructions on the screen and press <RETURN>. See figure Source Side Verification Setup.

Note

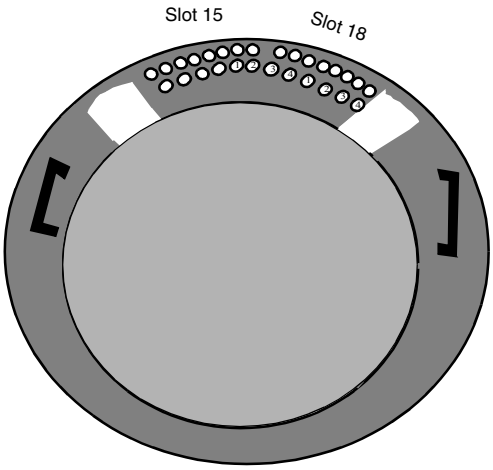
The figure Source Side Verification Setup shows DIB connections labeled by VNA slot and channel number.
Use this mapping to find the correct connection for the standalone source CV.
Source slot 19 appears in the same position as VNA slot 18 channel 2.
Source slot 20 appears in the same position as VNA slot 18 channel 3.

1) If the test passed, press <RETURN> and go back to step 2 of section UW6000 VNA Verification.
   If the test did not pass, recheck the connections, press <RETURN>, and go back to step 2 of the section UW6000 VNA Verification, and repeat the test on this source.



Source Side Verification Setup

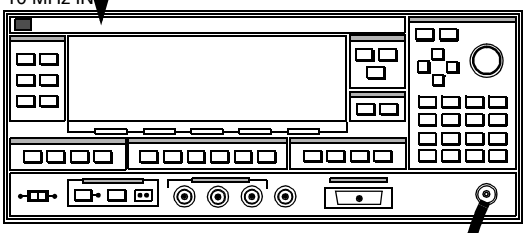
866-533-00 Microwave CV DIB



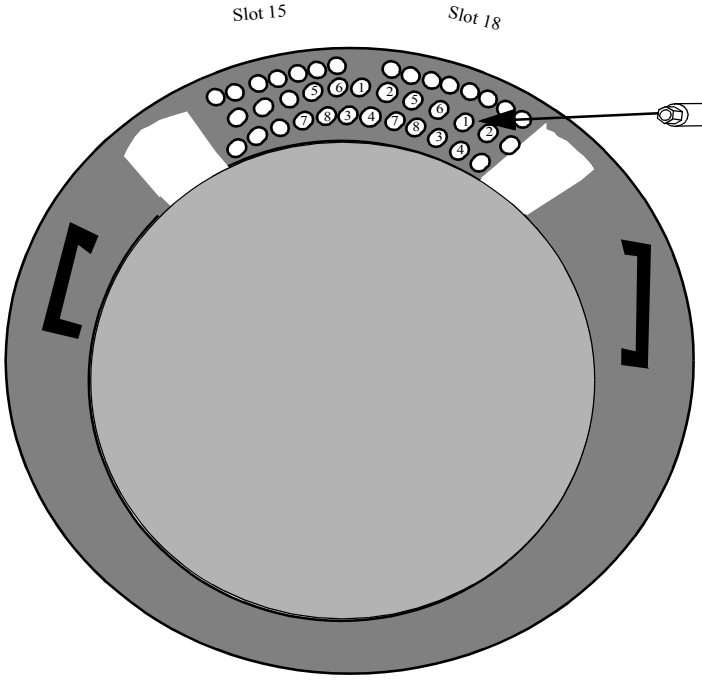
System 10 MHz Master Clock

10 MHz IN

HP 83623 Sweeper



866-532-00 Catalyst Microwave CV DIB

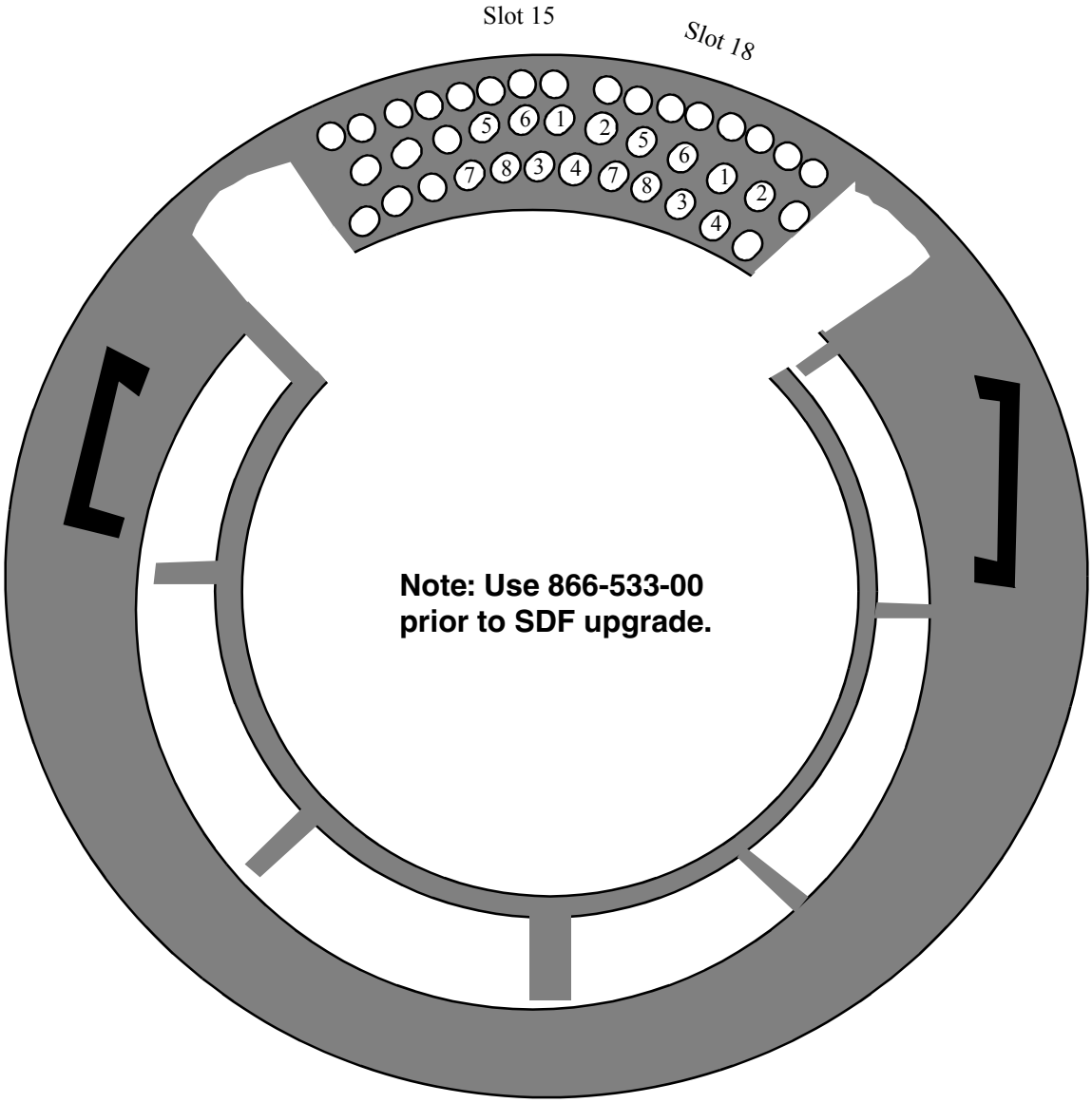


4 ft Coaxial Cable
SMA(f) to SMA(m)
with reinforced ends

Note: Use 866-533-00 prior to SDF upgrade.

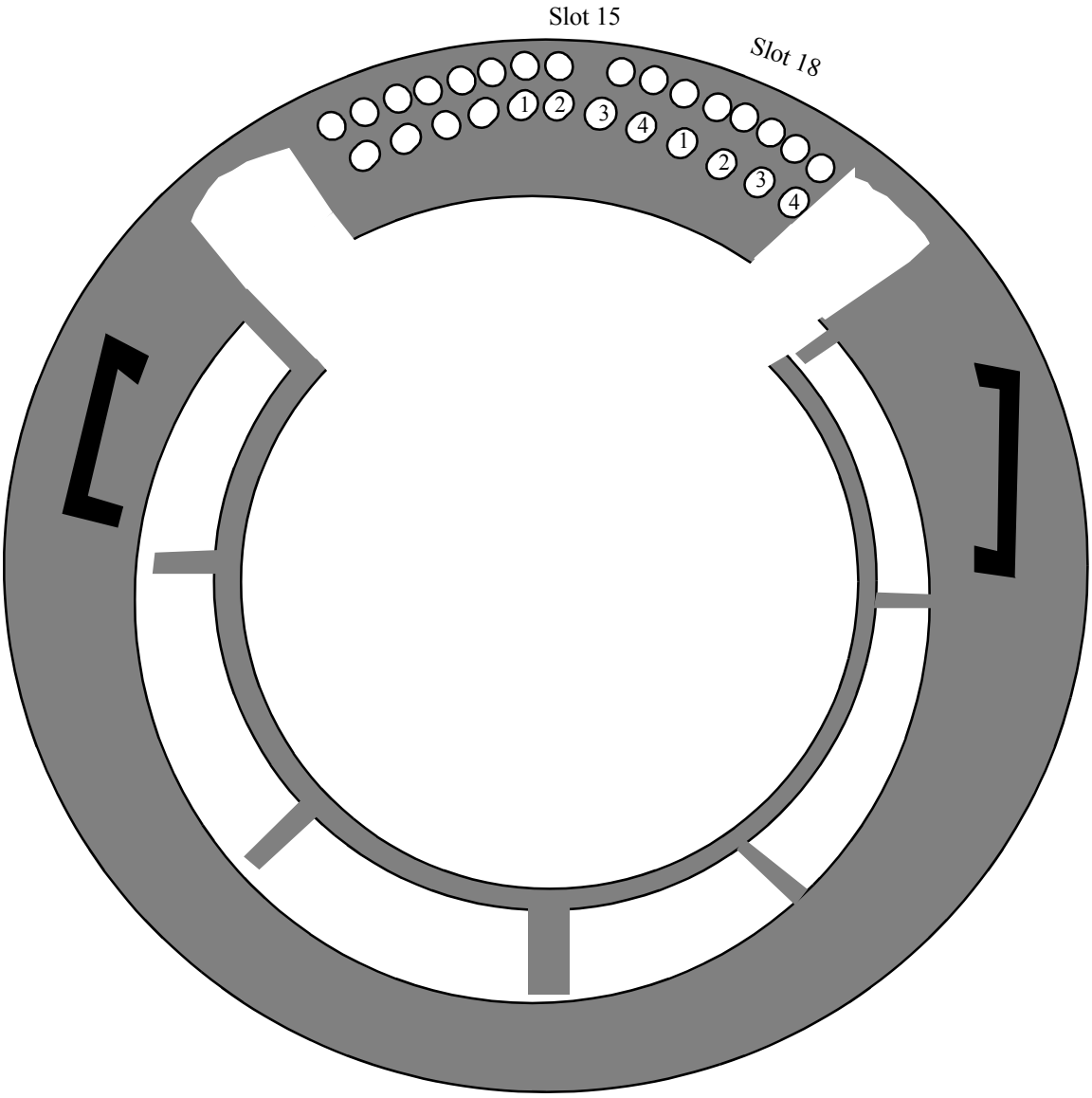
Receive Side Verification Setup

866-532-00 Catalyst Microwave CV DIB



Layout of the 866-532-00 CV DIB

866-533-00 Catalyst Microwave CV DIB



Layout of the 866-533-00 CV DIB

Overview

This chapter provides the specification support summaries for the:

- Internal Automatic Calibration - Occurs automatically at test program load time.
- Internal and External System Checkers - Invoked from the Checkers menu.
- External Calibration Procedures for Internal References - Performed at system output jacks by Maintenance Engineers using specified electronic test equipment.

Analog Pin Unit (APU) Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (calibrate -apu or job plan equivalent)

Weekly:

- Run catalyst_continuity_mi, apust, and matrixst in syscheck brief mode

Monthly:

- Run catalyst_continuity_mi, apust, and matrixst in syscheck full mode

Quarterly:

- Run apust in full mode
- Run matrixst in full mode
- Run catalyst_continuity_mi

Equipment Required

- Catalyst Continuity Kit (pn 806-166-00)

APU Calibration/Verification Description

The specifications of the APUs as described in the Catalyst Advanced Mixed-Signal Test System Specifications (pn 553-403-56) are maintained through the following programs.

Calibration

Table 4-1

Program	Purpose	Usage Interval
calibrate -dc	Autocalibration of DC subsystem	4 hours
calibrate -apu	Autocalibration of APU	4 hours
dcrefcal	DC reference calibration	90 days

Performance Test

Table 4-2

Program	Purpose	Usage Interval
dcst	Instrument performance test	1 week - brief mode 1 month - full mode
apust	Instrument performance test	1 week - brief mode 1 month - full mode
catalyst_continuity_mi	Connection performance test	1 week/90 days
matrixst	Connection performance test	1 week/90 days

Brief Summary of Each Program

calibrate -dc

Autocalibration is a process wholly internal to the system that compares the actual values of the DC source or voltmeter against standards located on the AD412 reference card. The transfer function of the source forcing and metering functions are evaluated for:

- Gain and offset - Voltage and current
- Linearity - Voltage only

The transfer functions of the meter inputs (vm1, vm2, and vmdif) are evaluated for:

- Gain and offset

calibrate -apu

APU calibration compares the actual values of the APU source or APU meter against standards located on the AD412 reference card. The transfer function of the APU forcing and metering functions are evaluated for:

- Gain and offset - Voltage and current

Corrections to the transfer functions are calculated and stored in memory.

dcrefcal

The dcrefcal calibration program uses an external meter, the HP 3458A, to measure and store the errors of the DC reference voltage sources and resistors located on the AD412 reference card. These errors are used to correct the reference values used during autocalibration. They are stored in an EEPROM on the reference card set. The calibration history of the DC reference can be extracted from the EEPROM and examined for stability.

dcst

The dcst calibration program checks all aspects of performance of the DC subsystem. The voltage and current, forcing and measuring functions are checked at several points per range usually including values that are not part of the calibration algorithm. The values are tested against the system references where appropriate, including points not directly related to calibration. Miscellaneous features and functions are also tested.

apust

The apust checker program checks performance of the APU. The voltage and current forcing and measuring functions are checked at several points per range, usually including values that are not part of the calibration algorithm. The values are tested against the system references where appropriate, including points not directly related to calibration. Miscellaneous features and functions are also tested.

catalyst_continuity_mi

The catalyst_continuity_mi checker program is designed to verify continuity (that is no opens or shorts) of all signals provided to the test head. The signals include matrix and DUT sources (force, sense, and guard), stored data bits, analog and digital instrument connections, and other miscellaneous signals. For a detailed description, review the Support Program Document (SPD) section of the catalyst_continuity_mi.tl source code located in the directory /image/ckr_bin.6.3 (or the latest version). The SPD is at the beginning of the file.

matrixst

The matrixst checker program tests the performance of the DC connections through the basic DC matrix. This includes testing for independence of all lines and pins, force and sense connections, and digital readback.

Traceability

The accuracy of the APU is based on a series of comparisons of instruments to references internal to the system. These references can be compared to external standards establishing a path to nationally accepted standards. This section describes the basic mechanisms that perform the comparison and verification of reference and instrument performance.

The path of comparison and verification is as follows:

- External standard to internal standard - dcrefcal
- Internal standard to instrument performance - autocalibration (calibrate -apu)
- Verification of autocalibration and instrument functionality - apust
- Verification of Path Performance
  Internal matrix - matrix_st
  Test head device area - catalyst_continuity_mi

External Standard to Internal Standard

The DC reference module (AD412 board) provides 14 voltage reference levels and five resistor references. These values are measured through external system connections using the dcrefcal program and the HP 3458A meter. Deviations from nominal value are stored for use by the autocalibration routines and checker programs.

Internal Standard to Intstrument Performance

APU calibration compares the forcing and measurement functions of the instruments to the reference values. Corrections to the transfer functions are stored in the executive software and used to modify the transfer functions at job run time. Bounds checking is performed on the transfer function corrections, but the overall calibration is performed open-loop. Verification of performance of the error-correction circuitry is performed in apust as explained in the following apust section.

All voltage and current calibrations are two-point fit to a line using averaging for best accuracy.

The voltage forcing functions are calibrated by measuring the differences between the forced values and the voltage references using the DC subsystem meter.

The voltage measurement functions are calibrated in the current forcing function. The difference of the read value is compared with the voltage reference. The current forcing functions are calibrated by forcing current through a reference resistor and comparing the voltage generated to a voltage reference using the DC subsystem meter.

Verification of Autocalibration and Instrument Functionality

The current measurement functions are calibrated by forcing voltage to the reference resistor. The difference of the read value is compared with the current calculated from output voltage and reference resistor.

The apust checker program provides verification of the performance of the hardware functionality and performance after calibration through measurements against the internal system references. In most cases, the verification uses a set of values.

Verification of Path Performance

Path performance is tested by two checkers: matrix_st and catalyst_continuity_mi. These checkers verify the independence of the force and sense connections and the integrity of the connections to the user area.

Advanced Time Measurement Subsystem (ATMS) Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (calibrate -tms)

Weekly:

- Run tmsalst in brief mode

Monthly:

- Run tmsalst in full mode

Annually:

- Run atms_cat_cv (optional to establish traceability)

Equipment Required for Optional Traceability Process

Refer to atms_cat_cv.

Advanced Time Measurement Subsystem (ATMS) Specification Support Description

Prior Conditions

In addition to the specified system warm-up and environmental conditions, the following conditions must be met before running ATMS autocalibration:

- DC subsystem reference calibration must be valid for ATMS autocalibration to be meaningful. (Refer to DC procedure dcrefcal Procedure.)
- Time master clock calibration must be valid for ATMS autocalibration to be meaningful. (Refer to frequency verification procedure tjd_cv.)

- DC subsystem autocalibration must be valid for ATMS autocalibration to run. (Refer to DC procedure DC Subsystem.)

ATMS Calibration / Verification Explanation

Table 5:

Program	Purpose	Usage Interval
calibrate -tms	Autocalibrate TMS	4 hours
tmsalst	Instrument Performance test	Weekly - brief mode Monthly - full mode
atms_cat_cv	External path length error performance test	Annually

Brief Summary of Each Program

calibrate -tms

Autocalibration is a system internal process that uses system time, voltage, and resistance references to determine the following ATMS parameters:

- Time interpolator transfer function
- Time base error
- Trigger level accuracy
- Time channel delay (electric path length)

These parameters are adjusted in job plan setup or measurement functions to put ATMS performance within specification.

tmsalst

The tmsalst checker program checks all aspects of ATMS performance. All features and specifications are tested using internal system references and techniques that are not related to the calibration algorithm. The path length error specifications for ATMS channels, while tested in tmsalst, use the same reference signal and path as the path length calibrator. Therefore external testing of path length error specifications is required.

atms_cat_cv

The atms_cat_cv checker program checks time channel delay or path length of each Catalyst tester channel. It uses the system user clock and TACH/ATMS as a fixed reference and measures the relative path length of every other tester channel registered with time measurement specifications.

Specification Support Summary

ATMS Features, Modes, Timer/Counter Functions

The ATMS tmsalst checker program checks functionality of all ATMS inputs, ranges, and modes listed in the ATMS section of the Catalyst System Specifications Manual (pn 553-403-56).

Time Base Error

Time base error is autocalibrated to the LA703 10 MHz master reference. The specification for the LA703 10 MHz reference can be found in the Catalyst System Specifications Manual (pn 553-403-56).

Time Measurement Accuracy and Time Channel Accuracy Relationships

The accuracy relationships are presented in the ATMS specification for informational purposes. They are intended to provide a guide for applying the ATMS specifications, but are not specifications.

Path Length Error

The ATMS tmsalst checker program measures the path length error of a path that is similar to the DUT connection. To be assured of ATMS compliance with the specification, an external calibration program, atms_cat_cv, will measure the residual path length error of each channel using an internal reference and external connection.

Jitter

The ATMS tmsalst checker program checks the jitter performance of each channel using an asynchronous input from the test head.

Analog Errors

The ATMS tmsalst checker program checks the analog performance of each ATMS channel using the calibrated DC subsystem input at the test head. The DC subsystem accuracy is more than an order of magnitude better than the specified ATMS performance.

Traceability

The accuracy of the ATMS is based on a series of comparisons of ATMS to internal system references. These references can be compared to external standards establishing a path to nationally accepted standards. This section describes the basic mechanisms that perform the comparison and verification of reference and instrument performance.

The path of comparison and verification is as follows:

- External standard to internal standard - dcrefcal
  - LA703 10 MHz master reference module calibration

- Internal standard to instrument performance - Autocalibration (calibrate -dc and calibrate -tms)
- Traceability of autocalibration - atms_cat_cv
- Instrument functionality - tmsalst

DC Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (calibrate -dc or job plan equivalent)

Weekly:

- Run catalyst_continuity_mi, dcst, and matrixst in syscheck brief mode

Monthly:

- Run catalyst_continuity_mi, dcst, and matrixst in syscheck full mode

Quarterly:

- Run dcrefcal
- Run dcst in full mode
- Run matrixst in full mode
- Run catalyst_continuity_mi

Equipment Required

Table 6:

Qty	Model/PN	Description
1	HP 3458A	Digital Multimeter
1	803-800-00	Level III Calibration Tool Kit

DC Calibration Specification Support

The DC specifications of the Catalyst advanced mixed signal test systems as described in the Catalyst Advanced Mixed-Signal Test System Specifications (pn 553-403-56) are maintained through the following programs:

Calibration

Table 4-1

Program	Purpose	Usage Interval
calibrate -dc	Autocalibration of DC subsystem	4 hours
dcrefcal	DC reference calibration	90 days

Performance Test

Program	Purpose	Usage Interval
dcst	Instrument performance test	1 week - brief mode 1 month - full mode
catalyst_continuity_mi	Connection performance test	1 month/90 days
matrixst	Connection performance test	1 week/90 days

Brief Summary of Each Program

calibrate -dc

Autocalibration is a process wholly internal to the system that compares the actual values of the DC source or voltmeter against standards located on the AD412 reference cards. The transfer function of the source forcing and metering functions are evaluated for:

- Gain and offset-Voltage and current
- Linearity-Voltage only

The transfer functions of the meter inputs (vm1, vm2, and vmdif) are evaluated for:

- Gain and offset

Corrections to the transfer functions are calculated and stored in memory.

dcrefcal

The dcrefcal calibration program uses an external meter, the HP 3458A, to measure and store the errors of the DC reference voltage sources and resistors located on the AD412 reference card. These errors are used to correct the reference values used during autocalibration. They are stored in an EEPROM on the reference card set. The calibration history of the DC reference can be extracted from the EEPROM and examined for stability.

dcst

The dcst checker program checks all aspects of performance of the DC subsystem. The voltage and current, forcing and measuring functions are checked at several points per range, usually including values that are not part of the calibration algorithm. The values are tested against the system references where appropriate, including points not directly related to calibration. Miscellaneous features and functions are also tested.

matrixst

The matrixst checker program tests the performance of the DC connections through the basic DC matrix. This includes testing for independence of all lines and pins, force and sense connections, and digital readback.

catalyst_continuity_mi

The catalyst_continuity_mi checker program is designed to verify continuity (that is no opens or shorts) of all signals provided to the test head. The signals include matrix and DUT sources (force, sense, and guard), stored databits, analog and digitial instrument connections, and other miscellaneous signals. For a detailed description, review the Support Program Document (SPD) section of the catalyst_continuity_mi.tl source code located in the directory /image/ckr_bin.6.3 (or the latest version). The SPD is at the beginning of the file.

Traceability

The accuracy of the DC subsystem is based on a series of comparisons of instruments to references internal to the system. These references can be compared to external standards establishing a path to nationally accepted standards. This section describes the basic mechanisms that perform the comparison and verification of reference and instrument performance.

The path of comparison and verification is as follows:

- External standard to internal standard - dcrefcal
- Internal standard to instrument performance - autocal
- Verification of autocalibration and instrument functionality - dcst
- Verification of path performance
  Internal matrix - matrix_st
  Test head device area - catalyst_continuity_mi

External Standard to Internal Standard

The DC reference module (AD412 board) provides 14 voltage reference levels and five resistor references.

These values are measured through external system connections using the dcrefcal program and the HP 3458A meter. Deviations from nominal value are stored for use by the autocalibration routines and checker programs.

Internal Standard to Instrument Performance

Autocalibration compares the forcing and measurement functions of the instruments to the reference values. Corrections to the transfer functions are stored in the executive software and used to modify the transfer functions at job run time. Bounds checking is performed on the transfer function corrections, but the overall calibration is performed open-loop. Verification of performance of the error correction circuitry is performed in dcst as explained in section Verification of Autocalibration and Instrument Functionality.

All voltage calibration, with the exception of the 0.5V, 50V, and 100V ranges, is performed using linear regression for determination of the transfer function errors. All other calibration uses a two-point fit to a line using averaging for best accuracy. Voltage forcing functions have a linearization calibration performed on the D/A converter. This calibration is ratio metric and does not require the use of an absolute standard.

The voltage forcing functions are calibrated by measuring the differences between the forced values and the voltage references using the DC subsystem meter.

The voltage measurement functions for the sources are calibrated simultaneously with the forcing function. The difference of the read value is compared with the known forced value. The voltage measurement function of the system meter is calibrated by direct measurement of the voltage reference levels.

The current forcing functions are calibrated by forcing current through a reference resistor and comparing the voltage generated to a voltage reference using the DC subsystem meter.

The current measurement functions are calibrated using the same method as the current forcing function.

Verification of Autocalibration and Instrument Functionality

The dcst checker program provides verification of the performance of the hardware functionality and performance after calibration through measurements against the internal system references. In most cases, the verification uses a set of values and/or test techniques different from the calibration algorithms to determine the performance of the instruments. The error correction circuitry for the transfer functions as well as the current set of transfer function corrections is tested.

Verification of Path Performance

Path performance is tested by two checkers: matrix_st and catalyst_continuity_mi. These checkers verify the independence of the force and sense connections and the integrity of the connections to the user area.

High-Current Unit (HCU) Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (calibrate -dc or job plan equivalent)

Weekly:

- Run catalyst_continuity_mi, hcust, and matrixst in syscheck BRIEF mode

Monthly:

- Run catalyst_continuity_mi, hcust, and matrixst in syscheck FULL mode

Quarterly:

- Run hcurefcal

Equipment Required

Table 5:

Qty	Model/PN	Description
1	HP 3458A	Digital multimeter
1	803-800-00	Catalyst Level III Tool Kit
1	806-166-00	Catalyst Continuity Kit

HCU Calibration/Verification Description

The HCU specifications, as described in the Catalyst Advanced Mixed-Signal Test System Specifications (pn 553-403-56) are maintained through the following programs.

Calibration

Table 4-1

Program	Purpose	Usage Interval
calibrate -dc	Autocalibration of DC subsystem	4 hours
dcrefcal	DC reference calibration	90 days
hcurefcal	HCU reference calibration	90 days

Performance Test

Table 4-2

Program	Purpose	Usage Interval
dcst	Instrument performance test	1 week - brief mode 1 month - full mode
hcust	Instrument performance test	1 week - brief mode 1 month - full mode
catalyst_continuity_mi	Connection performance test	1 week/90 days
matrixst	Connection performance test	1 week/90 days

Brief Summary of Each Program

calibrate -dc (HCU calibration)

Autocalibration is a process wholly internal to the system that compares the actual values of the HCU source or HCU meter against standards located on the AD412 reference card. The transfer function of the HCU forcing and measuring functions are evaluated for:

- Gain and offset - Voltage and current

dcrefcal

The dcrefcal calibration program uses an external meter, the HP 3458A, to measure and store the errors of the DC reference voltage sources and resistors located on the AD412 reference card. These errors are used to correct the reference values used during autocalibration. They are stored in an EEPROM on the reference card set. The calibration history of the DC reference can be extracted from the EEPROM and examined for stability.

hcurefcal

The hcurefcal calibration program uses an external meter to measure the errors of the reference resistors on the TJ151-00 HCU source analog board. These errors are used to correct the reference values used during autocalibration.

dcst

The dcst checker program checks all aspects of performance of the DC subsystem. The voltage and current, forcing and measuring functions are checked at several points per range, usually including values that are not part of the calibration algorithm. The values are tested against the system references where appropriate, including points not directly related to calibration. Miscellaneous features and functions are also tested.

hcust

The hcust checker program checks all aspects of performance of the HCU. The voltage and current forcing and measuring functions are checked at several points per range, usually including values that are not part of the calibration algorithm. The values are tested against the system references where appropriate, including points not directly related to calibration. Miscellaneous features and functions are also tested.

catalyst_continuity_mi

The catalyst_continuity_mi checker program is designed to verify continuity (that is, no opens or shorts) of all signals provided to the test head. The signals include matrix and DUT sources (force, sense, and guard), stored databits, analog and digitial instrument connections, and other miscellaneous signals. For a detailed description, review the Support Program Document (SPD) section of the catalyst_continuity_mi.tl source code located in the directory /image/ckr_bin.6.3 (or the latest version). The SPD is at the beginning of the file.

matrixst

The matrixst checker program matrixst tests the performance of the DC connections through the basic DC matrix. This includes testing for independence of all lines and pins, force and sense connections, and digital readback.

Traceability

The accuracy of the HCU is based on a series of comparisons of instruments to references internal to the system. These references can be compared to external standards establishing a path to nationally accepted standards. This section describes the basic mechanisms that perform the comparison and verification of reference and instrument performance.

The path of comparison and verification is as follows:

- External standard to internal standards - hcurefcal
- Internal standard to instrument performance - autocalibration (calibrate -dc)
- Verification of autocalibration and instrument functionality - dcst
- Verification of autocalibration and instrument functionality - hcust
- Verification of path performance
  Internal matrix - matrix_st
  Test head device area - catalyst_continuity_mi

External Standard to Internal Standard

The DC reference module (AD412 board) provides 14 voltage reference levels and five resistor references. These values are measured through external system connections using the dcrefcal program and the HP 3458A meter. Deviations from nominal value are stored for use by the autocalibration routines and checker programs. Current specifications for the 20 mA range are traceable via this reference.

The HCU source analog board and reference (TJ151-00) contains precision 100Ω, 10Ω, and 1Ω resistors that are used in autocalibration of the 200 mA and 2A ranges of the HCU. The program hcurefcal is used to establish the traceability of these references.

Internal Standard to Instrument Performance

Autocalibration compares the forcing and measurement functions of the instruments to the reference values. Corrections to the transfer functions are stored in the executive software and used to modify the transfer functions at job run time. Bounds checking is performed on the transfer function corrections, but the overall calibration is performed open-loop. Verification of performance of the error correction is performed in hcust as explained in the following section Verification of Autocalibration and Instrument Functionality.

All voltage and current calibration uses a three-point fit to a line using averaging for best accuracy.

The voltage forcing functions are calibrated by measuring the differences between the forced values and the voltage references using the DC subsystem meter.

The voltage measurement functions for the sources are calibrated simultaneously with the forcing function. The difference of the read value is compared with the known forced value. The current forcing functions are calibrated by forcing current through a reference resistor and comparing the voltage generated to a voltage reference using the DC subsystem meter.

The current measurement functions are calibrated using the same method as the current forcing function.

Verification of Autocalibration and Instrument Functionality

The hcust checker program, provides verification of the performance of the hardware functionality and performance after calibration through measurements against the internal system references.

Verification of Path Performance

Path performance is tested by two checkers: matrix_st and catalyst_continuity_mi. These checkers verify the independence of the force and sense connections and the integrity of the connections to the user area.

Note

The HCU calibration is part of the DC calibration. If an HCU is present, calibrate -dc performs both source and HCU calibration.

High-Speed Digital Specification Support Summary

Schedule

Daily:

- DC level and timing edge calibration.
- If autocalibration is enabled, the system monitors the system environment and will recalibrate as needed.
- If autocalibration is disabled, recalibration should be manually invoked whenever the ambient temperature varies by more than ± 3°C.

Weekly:

- Run system check in brief mode.
- Run the catalyst_continuity_mi checker as a stand-alone program, using default test coverage.

Monthly:

- Run system check in full mode.
- Run the catalyst_continuity_mi checker as a stand-alone program, using default test coverage:

Quarterly:

- Run the monthly programs.
- Run the catalyst_continuity_mi checker as a stand-alone program, enabling all tests.

Annually:

- Run the quarterly programs.
- Run the HSD calibration edge traceability, hsd_edge_cv.

Equipment Required for Optional Traceability and External Calibration Process

Refer to hsd_edge_cv.

The system warm-up and environmental conditions outlined in the system portion of the Catalyst System Specification Manual (pn 553-403-56) must be followed.

The DC subsystem and master frequency reference for the system must be in calibration.

HSD Calibration Explanation

Time base accuracy is calibrated through the LA703 10 MHz reference calibration. See LA703 10 MHz Master Reference Module Calibration Setup for more information.

DC/AC/Edge calibration is performed by running the hsd_st self-test checker in full mode. This verifies the channel specifications through internal connections. The path out to the DIB is verified by the catalyst_continuity_mi checker.

The calibration of channel-to-channel skew is performed by the start cal_set statement. This is executed at least once when the job is first loaded and then as needed after the first calibration is performed. Calibration can be triggered either manually or through the autocalibration procedure described in the IMAGE User Manual.

This calibration process uses an internal TDR subsystem distributed through a relay tree to calibrate the skew between each channel. The calibration is verified using the hsd_edge_cv process. This process measures the skew of all the HSD channels in each test head. This verifies the performance of the TDR subsystem, the relay tree, and the deskew process.

High Speed Digital Subsystem Traceability

Overview

DC specifications: The performance is verified by the Level II checkers. Each channel's per pin parametric unit (PPMU) is connected to the DC subsystem using the channel's internal matrix connection. DC levels, currents, and impedances are verified against the DC subsystem's instrumentation.

Dynamic specifications: The performance is verified by the Level II checkers. A series of measurements is made using the channel's driver and receiver. The dynamic performance is verified against the channel's DC specifications. The signal quality of the output path from the channel to the DIB is checked by the catalyst_continuity_mi_checker. This verifies continuity of the signal and ground connections.

Edge specifications: The performance of an individual channel is verified by the Level II checkers. A series of measurements is made using the channel's driver and receiver. These timing tests verify the edge performance against the system's frequency standard.

Timing Specification: The performance is verified by the Level IV process.

The timing edge specifications are calibrated by the calibrate -hsd process. This uses the internal TDR subsystem and relay tree. It aligns all the edges within the HSD subsystem to each other.

The performance of the edge calibration process is checked using external instrumentation. This verifies that the process is aligning the edges in the system properly. The process steps a digitizing oscilloscope from the output of a reference channel to all other channels, measuring the relative skew of each channel to the reference channel. The final result is a picture of the skew between all the channels in the system. This result is then tested against the accuracy specification. This process also verifies the dynamic performance of the channel path.

DC Specifications

The accuracy of the DC specifications is based on a series of measurements of each channel's performance against the DC subsystem. The accuracy of the DC subsystem is based on measurements of its performance against the DC system reference.

All channel card DC level specifications rely on calibration to achieve their accuracy.

The Verification path is external standard to internal standard.

Dynamic Specifications

Verification of the dynamic specifications of the HSD subsystem transfers the DC level accuracy specifications to dynamic measurements. Traceability is via the DC path described in section DC Specifications.

Timing Accuracy Specifications

Verification of the timing accuracy specifications of the HSD subsystem transfers the frequency/time accuracy specification of the LA703 10 MHz system frequency reference to the timing accuracy measurements. The accuracy of the frequency reference is based on measurements of its performance to an external standard.

All timing accuracy specifications rely on calibration to achieve their accuracy.

The path of comparison and verification is as follows:

- External standard to internal standard
  LA703 10 MHz system frequency reference calibration
  See section LA703 10 MHz Master Reference Module Calibration Setup for more information.
- Internal standard to instrument performance - Autocalibration (calibrate -hsd)
- Traceability of Autocalibration - hsd_edge_cv
- Instrument functionality
  System check (in full mode)
  catalyst_continuity_mi

Low-Frequency AC Specification Support Summary

Schedule

Weekly:

- Run lfacst and lfac_ams_st in brief mode
- Run catalyst_continuity_mi

Monthly:

- Run lfacst and lfac_ams_st in full mode

Annually:

- Run cat_lfac_cv process (required only for traceability)

Equipment Required for Optional Traceability Process

Refer to cat_lfac_cv.

Low-Frequency AC Specification Support Description

This section describes the specification support for the Low Frequency AC (LFAC) source and digitizer instrumentation. The procedure to support these instruments is contained in section External Calibration for Internal References (Level 3). The (LFAC) source and digitizer specifications are described in the Catalyst System Specification Manual (pn 553-403-56).

The specification support is broken up into two sections. The first section includes support for the general specifications for the LFAC source and digitizer listed in section 1 of the LFAC source and LFAC digitizer sections of the system specification manual. The second section supports the frequency range-dependent specifications of sine wave amplitude accuracy and the DC waveform linearity specifications of frequency range 1.

General Specifications

All specifications for the low frequency AC (LFAC) instrumentation require that no hardware or firmware adjustments be made to ensure performance. The frequency accuracy of the low frequency instrumentation is derived directly from the system RF synthesizer which serves as the time master clock for the system, and thus is the working frequency reference for the ac instrumentation.

Traceability for the LFAC instrumentation frequency accuracy is maintained by performing the recommended annual calibration of the LA703 10 MHz frequency reference as described in section LA703 10 MHz Master Reference Module Calibration Setup. Traceability of the guaranteed specifications is provided via support programs for the LFAC instrumentation. The general specifications that are guaranteed (excludes typical and nominal) include the DC specifications of the instrumentation and some of the frequency range-independent AC specifications.

Traceability of these specifications is maintained by following the support procedure for the DC subsystem as described in section DC Specification Support Summary. The traceable DC subsystem is then used to record the DC performance of the LFAC instrumentation. To periodically record the results of this check to aid in the record keeping for calibration, the LFACST program can be run with the system data logging function enabled to record the test results. It is recommended that lfacst be run weekly in brief mode and monthly in full mode to ensure full functionality of the LFAC instrumentation. The lfacst program through the use of the DC subsystem is used to record the performance for the following LFAC specifications:

LFAC Source

- Peak output voltage
- Waveform range and resolution
- Output current
- Output impedance

- Programmable DC baseline
- Overcurrent alarm detection threshold

LFAC Digitizer

- Input voltage range
- DC baseline removal
- Input impedance
- DC offset

Frequency Range-Dependent Specifications

The remaining frequency range-dependent specifications are supported by two levels of support procedures.

These two levels of specification support are to record the performance of the LFAC source and LFAC digitizer frequency range dependent specifications. The first is the lfacst checker, which should be run on the recommended basis. This program checks the AC frequency range dependent specifications by connecting each LFAC source to each LFAC digitizer via the test head THADS bus. In general, the lfacst program checks specification performance to test limits that equal the summation of the LFAC source and LFAC digitizer specifications. Since, in most cases, the LFAC source and LFAC Digitizer have very similar performance, the test limits for these tests in LFAC is approximately twice the instrumentation specification.

LFAC Traceability

The final level of specification support can be used to periodically record system performance to maintain specification traceability. If desired, an annual check can be performed by running the cat_lfac_cv process. This process uses an external HP 3458A multimeter and the LA723 PLF/LFAC PV DIB to record the performance of the LFAC instrumentation. These measurements provide traceability to national standards as long as the HP 3458A is periodically calibrated with traceable standards in accordance with the vendor's recommended calibration procedure.

The following specifications are traced using this procedure;

LFAC Source

- AC amplitude accuracy
- DC linearity
- DC offset

LFAC Digitizer

- AC amplitude accuracy
- Waveform linearity error
- Input linearity error
- DC offset

The cat_lfac_cv process uses the HP 3458A mulitmeter to record the sine wave amplitude accuracy, waveform linearity error, output linearity error, and DC offset of the LFAC source. The LFAC digitizer is connected in parallel with the HP 3458 to the LFAC source to measure its sine wave amplitude accuracy, waveform linearity error, input linearity error, and DC offset performance by comparing its measurements to the measurements made by the HP 3458. A datalog of both the source and digitizer performance can be generated while running this process to record the results.

Precision Low-Frequency Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (-autocal calibrate -plfsrc, -plfdig or job plan equivalent)

Note

IF -autocal is invoked in the job plan load file, PLF calibration will be automatically invoked by the system when required.

Weekly:

- Run plfalst, plf_ams_st in brief mode
- Run catalyst_continuity_mi

Monthly:

- Run plfalst, plf_ams_st in full mode

Annually:

- Run cat_plf_cv process (required only for traceability)

Equipment Required for Optional Traceability Process

See cat_plf_cv.

Precision Low Frequency Specification Support Description

This section describes the specification support for the precision low frequency (PLF) source and digitizer instrumentation. The procedures to support these instruments are contained in cat_plf_cv. The PLF source and digitizer specifications are described in the Catalyst System Specification Manual (pn 553-403-56).

The specification support is broken up into two sections. The first section includes support for the general specifications for the PLF source and digitizer listed in section 1 of the PLF source and PLF digitizer sections of the system specification manual. The second section supports the frequency range-dependent specifications of sine wave amplitude accuracy.

General Specifications

All specifications for the precision low-frequency (PLF) instrumentation require that no hardware or firmware adjustments be made to ensure performance. The frequency accuracy of the PLF instrumentation is derived directly from the system RF synthesizer which serves as the time master clock for the system, and thus is the working frequency reference for the AC instrumentation.

Traceability for the precision low-frequency (PLF) instrumentation frequency accuracy is maintained by performing the recommended annual calibration of the LA703 10 MHz frequency reference as described in section LA703 10 MHz Master Reference Module Calibration Setup. Traceability of the guaranteed specifications is provided via support programs for the PLF instrumentation.
The general specifications that are guaranteed (excludes typical and nominal) include the DC specifications of the instrumentation and some of the frequency range independent AC specifications. These specifications are completely checked to full specification (except PLFS DC Offset) using the DC subsystem in the plfalst checker program.

Traceability of these specifications is maintained by following the support procedure for the DC subsystem as described in section DC Specification Support Summary. The traceable DC subsystem is then used to record the DC performance of the PLF instrumentation. To periodically record the results of this check to aid in the record keeping for calibration, the plfalst program can be run with the system datalogging function enabled to record the test results. It is recommended that plfalst be run weekly in brief mode and monthly in full mode to insure full functionality of the PLF instrumentation. The plfalst program through the use of the DC subsystem is used to record the performance for the following PLF specifications:

PLF Source

- Peak output voltage
- Waveform range and resolution
- Output current
- Output impedance
- Programmable DC baseline
- Overcurrent alarm detection threshold

- Input voltage ranges
- DC baseline removal
- Differential input CMRR
- Waveform resolution
- Input impedance
- DC offset

Frequency Range-Dependent Specifications

The remaining frequency range-dependent specifications are supported by three levels of support procedures. The highest level is the plfsrc and plfdig autocalibration software that is resident with the system. Like other system autocalibration procedures, these are automatically invoked by the system when required.

The plfsrc autocalibration is used to periodically adjust the linearity of the 20-bit sigma-delta D/A converter in the mainframe. This is done by making a mainframe connection between the PLF source and the PLF digitizer. Calibration circuitry exists on the PLF source mainframe board such that only the uncalibrated performance of the PLF digitizer is required for the PLF source autocalibration to execute successfully. The linearity correction constants generated from this procedure are stored in a local memory on the PLF source mainframe board and are applied automatically during normal use of the PLF source.

PLF digitizer autocalibration uses a similar strategy. The PLF source and PLF digitizer are connected locally in the mainframe. Correction constants are generated for the linearity and internal loop gain of the sigma-delta A/D converter on the PLF digitizer mainframe. As with the PLF source, these constants are stored locally on the PLF digitizer mainframe board and are applied automatically during normal use of the PLF digitizer.

The above specifications are all that is required to periodically correct for any known error sources of the PLF source and PLF digitizer that are time or temperature dependent.

The other two levels of specification support are to record the performance of the PLF source and PLF digitizer frequency range-dependent specifications. The first is the plfalst checker, which should be run on the recommended basis. This program checks all of the AC frequency range-dependent specifications by connecting each precision low frequency source to each precision low frequency digitizer via the test head THADS bus. In general, the plfalst program checks specification performance to test limits that equal the summation of the PLF source and PLF digitizer specifications. Since, in most cases the PLF source and PLF digitizer have very similar performance, the test limits for these tests in plfalst is approximately twice the instrumentation specification.

PLF Traceability

The final level of specification support can be used to periodically record system performance to maintain specification traceability. If desired, an annual check can be performed by running the cat_plf_cv process. This process uses an external HP 3458A multimeter and the LA723 PLF CV DIB to record the performance of the PLF instrumentation. These measurements provide traceability to national standards as long as;

- The HP 3458A is periodically calibrated with traceable standards in accordance with the vendor's recommended calibration procedure.

The following specifications are traced using this procedure;

PLF Source

- AC amplitude accuracy
- DC linearity error
- DC offset
- DC offset drift

PLF Digitizer

- AC amplitude accuracy
- Waveform linearity error
- Input linearity error
- DC offset
- DC offset drift

The cat_plf_cv process uses the HP 3458A multimeter to record the sine wave amplitude accuracy, waveform linearity error, output linearity error, DC offset and DC offset drift of the PLF source. The PLF digitizer is connected in parallel with the HP 3458 to the PLF source to measure its sine wave amplitude accuracy, waveform linearity error, input linearity error, and DC offset drift performance by comparing its measurements to the measurements made by the HP 3458 meter. A datalog of both the source and digitizer performance can be generated while running this process to record the results.

PMM Specification Support Summary

Schedule

Every 24 hours:

- Run autocalibration (calibrate -pmm -dcv -acv -ohms or job plan equivalent).

Weekly:

- Run catalyst_continuity_mi and pmmst in syscheck brief mode.

Monthly:

- Run catalyst_continuity_mi and pmmst in syscheck full mode.

Quarterly or annually (See note below):

- Run pmm_xcal_mi.

Note

The PMM instrument specification is time dependent. Teradyne provides specification details at quarterly and annual intervals. Consult the PMM specifications to determine the instrument performance accuracy and match the appropriate calibration period with the test accuracy requirements.

Equipment Required

Refer to pmm_xcal_mi Procedure.

PMM Calibration Specification Support

The specifications of the PMM as described in the Catalyst Advanced Mixed-Signal Test System Specifications (pn 553-403-56) are maintained through the following programs:

Calibration

Table 4-3

Program	Purpose	Usage Interval
calibrate -pmm -dcv -acv -ohms	Autocalibration of DC subsystem	24 hours
pmm_xcal_mi	PMM reference calibration	90 days

Performance Test

Table 4-4

Program	Purpose	Usage Interval
pmmst	Instrument performance test	1 week - brief mode 1 month - full mode
catalyst_continuity_mi	Connection performance test	1 week
catalyst_continuity_mi	Connection performance test	1 month

Brief Summary of Each Program

calibrate -pmm -dcv -acv -ohms

Autocalibration is a process internal to the PMM's HP 3458A meter that calibrates each meter range and function by comparing their performance against standards located in the meter. Run time is approximately 12 minutes.

pmm_xcal_mi

The pmm_xcal_mi calibration program uses an external 10V DC voltage standard (Datron 4910) and external 10K resistor standard (Fluke 742A-10K) to measure and store the errors of the DC reference voltage source and resistor located in the HP 3458A meter. These errors are used to correct the reference values used during autocalibration. The program pmm_xcal_mi also autocalibrates the HP 3458A meter and creates a record file of the calibration named pmm_cal_record in the current directory. If there is an existing pmm_cal_record file, the new data is appended to it.

pmmst

The pmmst checker program checks all aspects of performance of the PMM. The voltage and current measuring functions are checked at several points per range against the system sources. Miscellaneous features and functions are also tested.

catalyst_continuity_mi

The catalyst_continuity_mi checker program tests the continuity of the pmm path to the area of the device interface board (DIB).

Traceability

The accuracy of the PMM is based on a series of comparisons to references internal to the HP 3458A meter. These references can be compared to external standards establishing a path to nationally accepted standards. This section describes the basic mechanisms that perform the comparison and verification of reference and instrument performance.

The path of comparison and verification is as follows:

- External Standard to Internal Standards - pmm_xcal_mi
- Internal Standard to Instrument Performance - autocalibration (calibrate -pmm)
- Verification of Autocalibration and Instrument Functionality - pmmst
- Verification of Path Performance to Test Head Device Area - catalyst_continuity_mi

External Standard to Internal Standard

The HP 3458A meter provides one voltage reference and one resistor reference. The program pmm_xcal_mi compares these values against an external 10V DC voltage standard (Datron 4910) and an external 10K resistor standard (Fluke 742A-10K). Deviations from nominal values are stored in the HP 3458A meter for use by the autocalibration routines.

Autocalibration compares the measurement functions of the HP 3458A meter to its reference values. Corrections to the transfer functions are stored in the HP 3458A meter's internal software and are used to modify the transfer functions. Refer to the HP 3458A Manual for more information.

The checker program, pmmst, provides verification of the performance of the hardware functionality and performance after calibration through measurements against the internal system references.

Path performance is tested by checker catalyst_continuity_mi. This checker verifies the integrity of the pmm connections to the user area.

Very High-Frequency Arbitrary Waveform Generator Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (calibrate -vhfawg or job plan equivalent).

Weekly:

- Run vhfst in brief mode
- Run catalyst_continuity_mi

Monthly:

- Run vhfst in full mode

Annually:

- Run the vhfawg_cv process (required only for traceability).

Equipment Required for Optional Traceability Process

Refer to vhfawg 1200 cv and vhfawg400 diff cv.

Very High Frequency Arbitrary Waveform Generator Specification Support Description

This section describes the specification support for the very high frequency arbitrary waveform generator (VHFAWG400 DIFF and VHFAWG1200) Instrument Family. The procedures to support these instruments are contained in vhfawg 1200 cv and vhfawg400 diff cv. The VHFAWG400 DIFF and VHFAWG1200 specifications are described in the appropriate section of the Catalyst System Specification Manual (pn 553-403-56). The specification support is broken up into two sections. The first section includes support for the general specifications for the VHFAWG400 DIFF and VHFAWG1200. The second section supports the frequency range-dependent specifications of sine wave level accuracy.

All specifications for the VHFAWG400 DIFF and VHFAWG1200 require that no hardware or firmware adjustments be made to ensure performance. The frequency accuracies of the VHFAWG400 DIFF and VHFAWG1200 are derived directly from the RF synthesizer, which serves as the time master clock for the system, and thus the working frequency reference for the AC instrumentation. Traceability of this reference is maintained by performing the recommended annual calibration of the system LA703 10 MHz frequency reference as described in section LA703 10 MHz Master Reference Module Calibration Setup.

General Specifications

Traceability of the guaranteed specifications is provided via support programs for the VHFAWG400 DIFF and VHFAWG1200. The general specifications that are guaranteed (excludes typical and nominal) include the DC specifications of the instrumentation. These specifications are completely checked to full specification using the DC subsystem in the vhfst checker program.

Traceability of these specifications is maintained by following the support procedure for the DC subsystem as described in DC Specification Support Summary. The traceable DC subsystem is then used to record the DC performance of the VHFAWG400 DIFF and VHFAWG1200. To periodically record the results of this check and to aid in the record keeping for calibration, the vhfst program can be run with the system datalogging function enabled to record the test results.

It is recommended that vhfst be run weekly in brief mode and monthly in full mode to ensure full functionality of the VHFAWG400 DIFF and VHFAWG1200. The vhfst program through the use of the DC subsystem is used to record the performance for the following VHFAWG400 DIFF and VHFAWG1200 specifications:

- Peak output voltage
- Waveform range and resolution
- Output current
- Programmable DC baseline
- Waveform resolution

Frequency Range-Dependent Specifications

The remaining frequency range-dependent specifications are supported by three levels of support procedures. The highest level is the autocalibration processes of leveling and fine attenuation calibration. These processes are invoked automatically by the system when required as with all system autocalibration functions. The process of leveling is the calibration of the frequency response errors of the VHFAWG400 DIFF and VHFAWG1200 signal paths. Here, the user's operating point is leveled using a frequency response standard resident in the VHFAWG400 DIFF and VHFAWG1200 channel cards.

The absolute accuracy of this curve is also calibrated periodically by comparing an operating point against a temperature-independent absolute level reference oscillator, also resident on the VHFAWG400 DIFF and VHFAWG1200 channel cards. The fine attenuation calibration consists of a linearization of the fine attenuation circuitry in the VHFAWG400 DIFF and VHFAWG1200 mainframes by comparing their attenuation curves against the precision step attenuators on the VHFAWG400 DIFF and VHFAWG1200 channel cards.

The other two levels of specification support procedures for the frequency range-dependent specifications are used to record performance. Again, on the above recommended periodic basis, the vhfst checker should be run. This program checks all of the AC frequency range-dependent specifications by connecting each VHFAWG400 DIFF and VHFAWG1200 to a VHF digitizer via the test head THADS bus.

In general, the vhfst program checks specification performance to test limits that equal the summation of the VHFAWG400 DIFF and VHFAWG1200 and VHF digitizer specifications.

Since, in most cases, the VHFAWG400 DIFF and VHFAWG1200 and VHF digitizer have very similar performance, the test limits for these tests in vhfst is approximately twice the instrumentation specification.

VHFAWG400 DIFF and VHFAWG1200 Traceability

The final level of specification support can be used to periodically record full system performance to maintain specification traceability. If desired, an annual check can be performed by running the vhfawg_400diff or vhfawg_1200 process. These processes use external instrumentation that, when supported with the vendor's recommended calibration procedures via traceable measurements, provides a traceability path for the following AC specifications of the VHFAWG400 DIFF and VHFAWG1200:

- Absolute level accuracy
- Step attenuation relative accuracy

The vhfawgcv processes use an external instrument to record the performance of the VHFAWG400 DIFF and VHFAWG1200. The program will guide the operator through the process with instructions that appear on the test system's user computer workstation.

A datalog of the VHFAWG400 DIFF and VHFAWG1200 performance can be generated while running this process to record the results.

Very High Frequency Continuous Wave Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (calibrate -vhfcw or job plan equivalent).

Weekly:

- Run vhfst in brief mode.
- Run continuity checks

Monthly:

- Run vhfcwst in full mode.

Annually:

- Run the vhfcw_cv process (only required for traceability)

Equipment Required for Optional Traceability Process

Refer to vhfcw_cv.

Very High-Frequency Continuous Wave Specification Support Description

This section describes the specification support for the very high frequency continuous wave (VHFCW). The procedure to support this instrument is contained in vhfcw_cv. The specifications are described in the appropriate section of the Catalyst System Specification Manual (pn 553-403-56). The specification support is broken up into two sections. The first section includes support for the general specifications for the VHFCW. The second section supports the frequency range dependent specifications of sine wave level accuracy, sine wave harmonics, and sine wave spurious responses.

All specifications for the VHFCW require that no hardware or firmware adjustments be made to ensure performance. The frequency accuracy of the VHFCW is derived directly from the RF synthesizer, which serves as the time master clock for the system, and thus is the working frequency reference for the AC instrumentation. Traceability of this reference is maintained by performing the recommended annual calibration of the system LA703 10 MHz frequency reference as described in section LA703 10 MHz Master Reference Module Calibration Setup.

General Specifications

Traceability of the guaranteed specifications is provided via support programs for the VHFCW. The general specifications that are guaranteed (excludes typical and nominal) include the DC specifications of the instrumentation. These specifications are completely checked to full specification using the DC subsystem in the vhfcwst checker program.

Traceability of these specifications is maintained by following the support procedure for the DC subsystem as described in section DC Specification Support Summary. The traceable DC subsystem is then used to record the DC performance of the VHFCW. To periodically record the results of this check and to aid in the record keeping for calibration, the VHFCWST program can be run with the system datalogging function enabled to record the test results.

It is recommended that vhfcwst be run weekly in brief mode and monthly in full mode to ensure full functionality of the VHFCW. The vhfcwst program through the use of the DC subsystem is used to record the performance for the following VHFCW specifications:

- Peak output voltage
- Waveform range and resolution
- Output current
- Programmable DC baseline
- Waveform resolution

Frequency Range Dependent Specifications

The remaining frequency range-dependent specifications are supported by three levels of support procedures. The highest level is the autocalibration processes of leveling and fine attenuation calibration. These processes are invoked automatically by the system when required as with all system autocalibration functions. The process of leveling is the calibration of the frequency response errors of the VHFCW signal path. Here, the user's operating point is leveled using a frequency response standard resident in the VHFCW channel card.

The absolute accuracy of this curve is also calibrated periodically by comparing an operating point against a temperature-independent absolute level reference oscillator, also resident on the VHFCW channel card. The fine attenuation calibration consists of a linearization of the fine attenuation circuitry in the PTS250 by comparing its attenuation curve against the precision step attenuators on the VHFCW channel card.

The other two levels of specification support procedures for the frequency range-dependent specifications are used to record performance. The vhfcwst checker should be run according to section Schedule. This program checks all of the AC frequency dependent specifications by connecting each VHFCW to a TMS via the test head THADS bus.

Testing output level is done by using the leveling diode detector on the VHFCW channel card and DC subsystem via the measure bus.

VHFCW Traceability

The final level of specification support can be used to periodically record full system performance to maintain specification traceability. If desired, an annual check can be performed by running the vhfcw_cv process. This process uses external instrumentation that, when supported with the vendor's recommended calibration procedures via traceable measurements, provides a traceability path for the following:

- Absolute level accuracy
- Step attenuation relative accuracy

The vhfcw_cv process uses an HP 8902 measurement receiver to record the absolute sine wave accuracy performance at the level calibration point, +10 dBm, and the relative accuracy of the channel card step attenuators to record all error sources of sine wave amplitude accuracy. The program guides the operator through the process with instructions that appear on the test system's user computer workstation. A datalog of the VHFCW performance can be generated while running this process to record the results.

Very-High Frequency Digitizer Specification Support Summary

Schedule

Every 4 hours:

- Run autocalibration (calibrate -hfdig or job plan equivalent)

Weekly:

- Run vhfst in brief mode.
- Run catalyst_continuity_mi

Monthly:

- Run vhfst in full mode.

Annually:

- Run the vhfd_cv process (only required for traceability).

Equipment Required for Optional Traceability Process

Refer to VHF Digitizer CV.

Very High-Frequency Digitizer Specification Support Description

This section describes the specification support for the very high-frequency digitizer (VHFD). The procedure to support this instrument is contained in section VHF Digitizer CV. The VHFD specifications are described in the appropriate section of the Catalyst System Specification Manual (pn 553-403-56). The specification support is broken up into two sections. The first section includes support for the general specifications for the VHFD. The second section supports the frequency range-dependent specification of sine wave level accuracy.

All specifications for the VHFD require that no hardware or firmware adjustments be made to ensure performance. The frequency accuracy of the VHFD is derived directly from the RF synthesizer, which serves as the time master clock for the system and, thus is the working frequency reference for the AC instrumentation. Traceability of this reference is maintained by performing the recommended annual calibration of the system LA302 10 MHz frequency reference as described in section LA703 10 MHz Master Reference Module Calibration Setup.

General Specifications

Traceability of the guaranteed specifications is provided via support programs for the VHFD. The general specifications that are guaranteed (excludes typical and nominal) include the DC specifications of the instrumentation. These specifications are completely checked to full specification using the DC subsystem in the vhfst checker program.

Traceability of these specifications is maintained by following the support procedure for the DC subsystem as described in DC Specification Support Summary. The traceable DC subsystem is then used to record the DC performance of the VHFD. To periodically record the results of this check and to aid in the record keeping for calibration, the vhfst program can be run with the system datalogging function enabled to record the test results.

It is recommended that vhfst be run weekly in brief mode and monthly in full mode to ensure full functionality of the VHFD. The vhfst program through the use of the DC subsystem is used to record the performance for the following VHFD specifications:

- Sample rate range
- Sampling resolution
- Time measurement access
- Input impedances and voltages
- DC offset performance
- Filter specifications
- IF sine wave distortion

The vhfst checker checks all of the AC frequency dependent specifications by connecting each VHFD to a very high frequency arbitrary waveform generator (VHFAWG) via the test head THADS bus.

Since in most cases the VHFD and VHFAWG have very similar specification performance, the test limits for these tests in vhfst up to 10 MHz will be approximately twice the instrumentation specification.

Frequency Range-Dependent Specifications

The remaining frequency range-dependent specifications are supported by three levels of support procedures.

The first and most frequent step in obtaining calibrated measurements requires executing the VHFD calibration program, which is typically done at runtime, prior to instrument use. In most cases, the calibration program is run automatically by IMAGE after user program load-time, system initialization, or every 4 hours thereafter.

This step is referred to as error measurement. A highly accurate and repeatable reference AC voltage is produced by the broadband calibration source (BCS), which resides on the channel card itself and is measured by the VHFD over a range of measurement modes. Error is calculated based on expected versus measured signal levels. The error correction takes place at the instrument's FIR filter, where the signal is multiplied by the appropriate correction factor. This is part of the process known as data correction.

The second level of support is achieved through regular iterations of the vhfst program. The checker should be run weekly in brief mode and monthly in full mode.

VHFD Traceability

The final level of specification support can be used to periodically record full system performance to maintain specification traceability. If desired, an annual check can be performed by running the vhfd_cv process. This process uses external instrumentation that when supported with the vendor's recommended calibration procedures via traceable measurements, provides a traceability path for the following specifications of the VHFD:

- Amplitude accuracy

The vhfd_cv process serves to maintain the VHFD amplitude accuracy traceability by performing a set of amplitude accuracy tests. This set of amplitude tests is defined by the specifications called out in the ESSD. CV test point selection is optimized for maximum coverage in all specified frequency and voltage ranges while minimizing redundancy in test coverage.

The vhfd_cv process uses two external instruments to stimulate and measure the performance of the VHFD. The program will guide the operator through the process with instructions that appear on the test system's user computer workstation. An HP8902 measurement receiver is used to record the sine wave amplitude accuracy performance, while an HP8657 provides an input signal. A datalog of the VHFD performance can be generated while running this process to record the results. See section VHF Digitizer CV for more detail.

UW6000 Specification And Support Summary

Schedule

- Every 4 hours - Run autocalibration, which contains the following checkers: uhfsrc, uwsrc, uwport, uwrecv, or job plan equivalent.
- Weekly - Run the following checkers: uhfcwst, uwst, modsrcst in BRIEF mode. Run the catalyst_continuity checker.
- Monthly - Run the following checkers: uhfcwst, uwst, and modsrcst in FULL mode. Run the uwmi and modsrc_mi checkers.
- Annualy - Run the uw6000_cv process (only required for traceability).

Equipment Required for Optional Traceability

Refer to Section 3 of the uw6000_cv process.

UW6000 Specification Support Description

The UW6000 specifications are qualified at the customers site using calibrations levels 1, 2 and 4. Level 1 performs the internal auto-calibration. Functionality and ESSD verification is tested using the uhfcwst, uwst, and modsrcst checkers in Level 2. Traceability for these specifications is provided in Level 4 using calibrated external instruments. Note, there is no level 3 test to be performed for this option.

Qualification for each level requires that no hardware or firmware adjustments are made to ensure proper performance. Since each new level is progressively more comprehensive than the last, the qualification of the higher calibration levels depend on the passing qualification of their dependent lower calibration levels. This is also true of the individual tests contained within a single calibration level.

Level 1: Internal Calibration

Level 1 performs the auto-calibration process to calibrate the power level and attenuation of the UW6000 Microwave Options. This process is automatically invoked by the system, like all system auto-calibration functions, when activated by typing -autocal on the command line. The systems autocalibration process is preferred over individually calibrating each instrument because the autocalibration was designed to calibrate each instrument in the order of their dependencies on other instruments so as to ensure proper qualification.

The process of calibrating the power level and attenuation is done by measuring the output signal, via internal diode detectors, with the DC sub system. The measurement is then compared to the reference value stored in the source and uwport channel cards. The difference between the measurement and the reference value, referred to as the error term is then used to re-calibrate the source and bring the output signal back to specification. This illustrates the importance of calibrating the DC subsystem first before calibrating the UW6000 Microwave Option. This process is performed across the entire frequency band of the source using incremental frequency steps.

Level 2: Checkers

Functionality and verification of the guaranteed specifications is provided by the uhfcwst, uwst, uwmi, modsrcst, and modsrc_mi checkers. The guaranteed specifications exclude any and all specifications labeled as typical or nominal as well as any specifications that are derived from the guaranteed specifications. Traceability of the guaranteed specifications is accomplished internally through the DC subsystem, VHF Digitizer, and the systems internal 10 MHz clock. The traceable DC of these instruments is used to record the performance of the UW6000 Microwave Options.

It is recommended that the uhfcwst, uwst, and modsrcst checkers be run weekly in BRIEF mode and monthly in FULL mode to ensure full functionality of the UW6000 Option. Internal verification is accomplished through the uwmi and modsrc_mi checkers and should be run monthly. To periodically record the results of these checks and to aid in the record keeping of this calibration level, the uhfcwst, uwst, and the uwmi programs can be run with the system datalog function enabled. These programs through the use of the DC subsystem, VHF Digitizer, and internal checker board are used to record the performance for the following UW6000 source specifications:

- Output Level

- Band SwitchingSpectral Purity
- Frequency and Level Switching Time
- Receive Level
- Detector Output
- IF Flatness
- Noise Source Option

Level 3: System Reference

There are no system references that need to be calibrated for the UW6000 Microwave options.

Level 4: Traceability

Traceability is the final level of specification support. Here, the traceable path is defined externally through customer or vendor owned bench top instrumentation that undergoes periodic calibration. The uw6000_cv program will guide the operator through the UW6000 CV process with instructions that appear in the station window. The HP E4418 Power Meter is used to record the 5 dB absolute amplitude of the source output. There the 5dB absolute amplitude point is the known reference point from which all the source side specifications of the UW6000 Microwave Option are derived. The HP 83623 Synthesized Sweeper is used to record the receive side measuring specifications that are referenced at 0 dBm. A datalog of the uw6000_cv results can be generated while running this process.

Appendix A
Device Interface Board (DIB) Interfacing Details

LA785 DIB Interface Description

The LA785 Multipurpose CV DIB provides high-performance connection access to all analog and digital test system instrumentation. All signals are connected from the test head cardlets to the Device Interface using a common 2-pin header interface. Connection to the 2-pin headers are made using a high-performance, coaxial, SMA-to-2-pin header cable (pn 807-322-00).

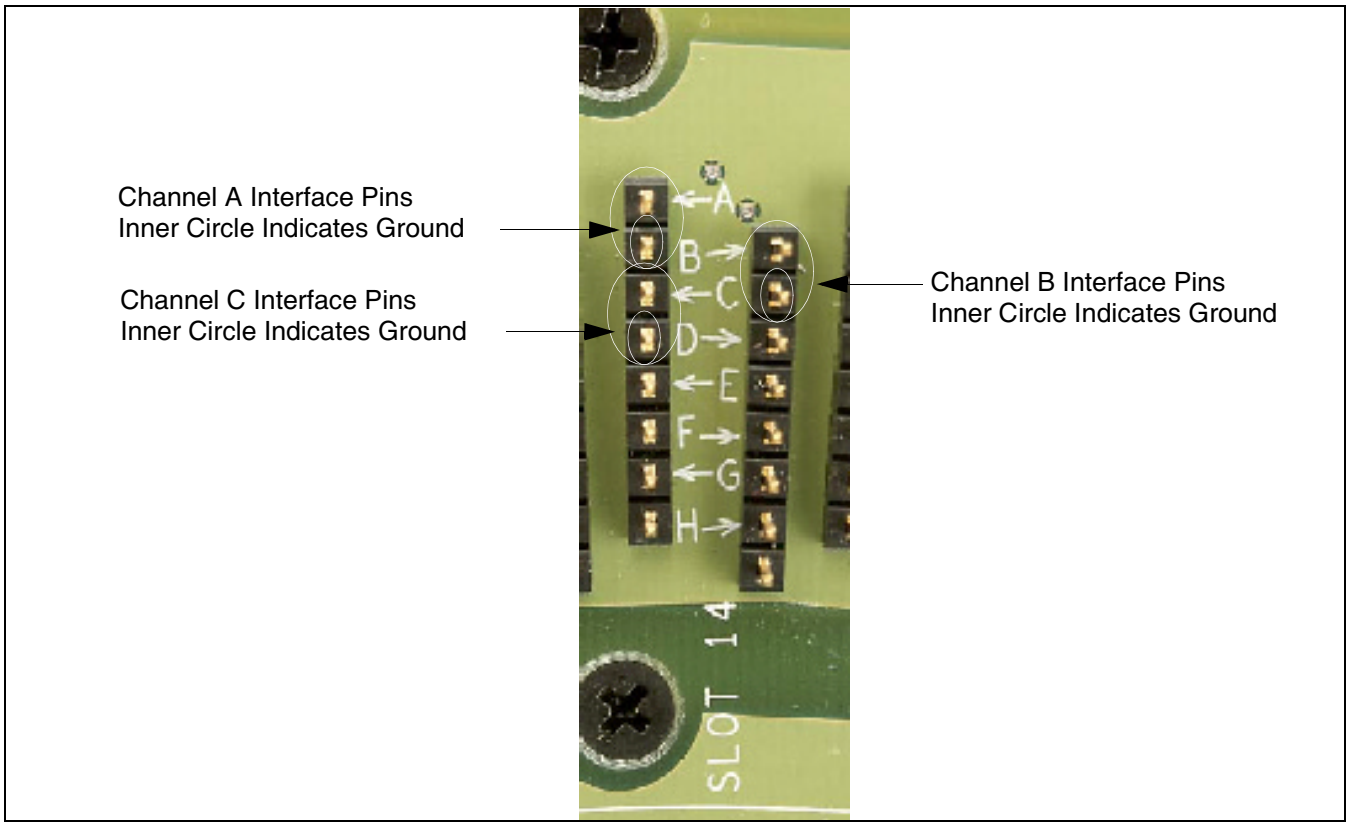
Ground Signals

The LA785 DIB design is such that all ground signals are common. The base DIB printed circuit board design sections grounds into analog, digital, and test head ground plane signals. Jumper connections are then installed on the board that ties all ground planes together.

Analog Instruments

Analog instrument interfacing is accomplished on a slot basis, with each slot offering eight channels. The channels are identified as A to H. Each channel has an accompanying ground signal. (For more information on ground signals, see section Ground Signals.)

The figure LA785 Analog Channel Interface Pins provides a magnified view of one of the analog slots. Interfacing to each of the eight signals is performed by connecting the cable (pn 807-322-00) to the appropriate pair of header pins. Note that the coaxial cable (pn 807-322-00) provides a white dot on the 2-pin header housing. This dot indicates the location of the outer conductor of the cable. The outer conductor (or shield) must always be connected to a DIB ground signal. The LA785 DIB silk-screen information provides the slot number and pin location of the signal (center conductor).

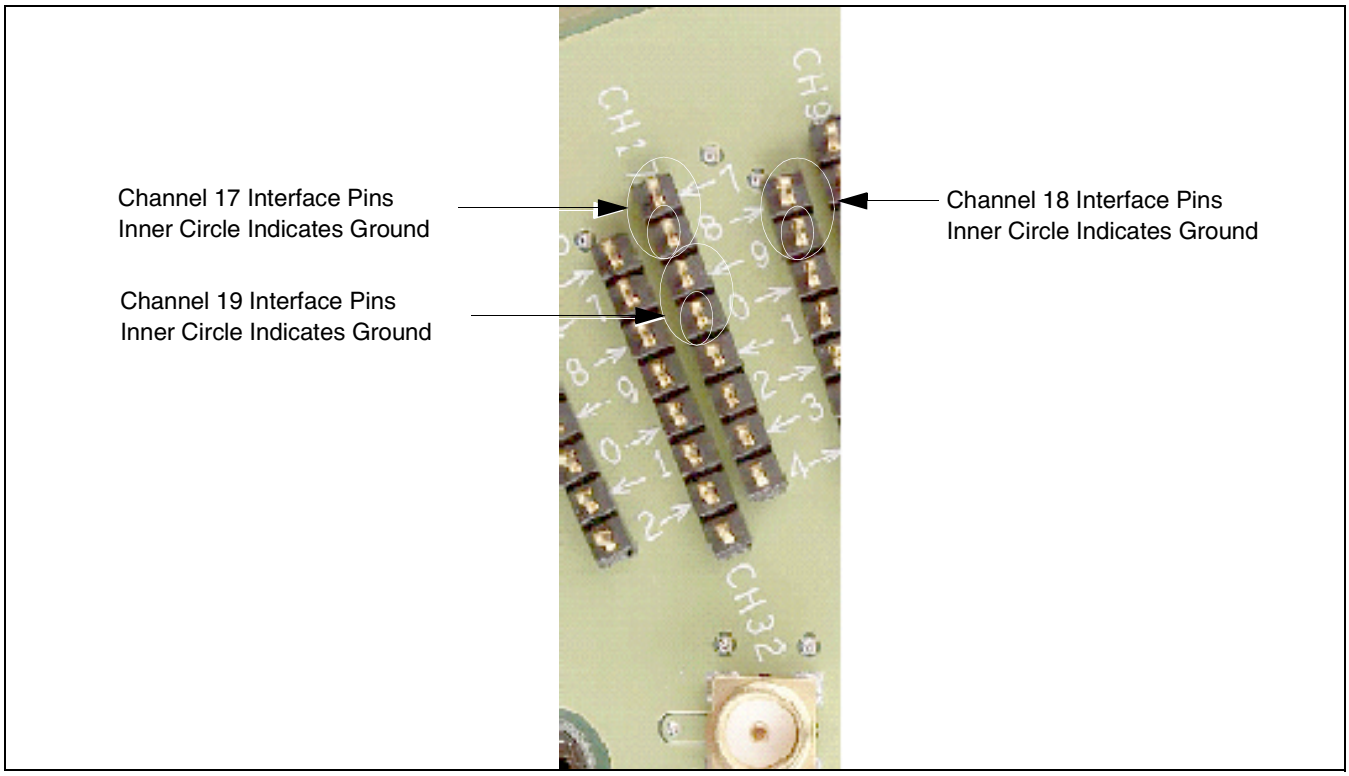


LA785 Analog Channel Interface Pins

Digital Instruments

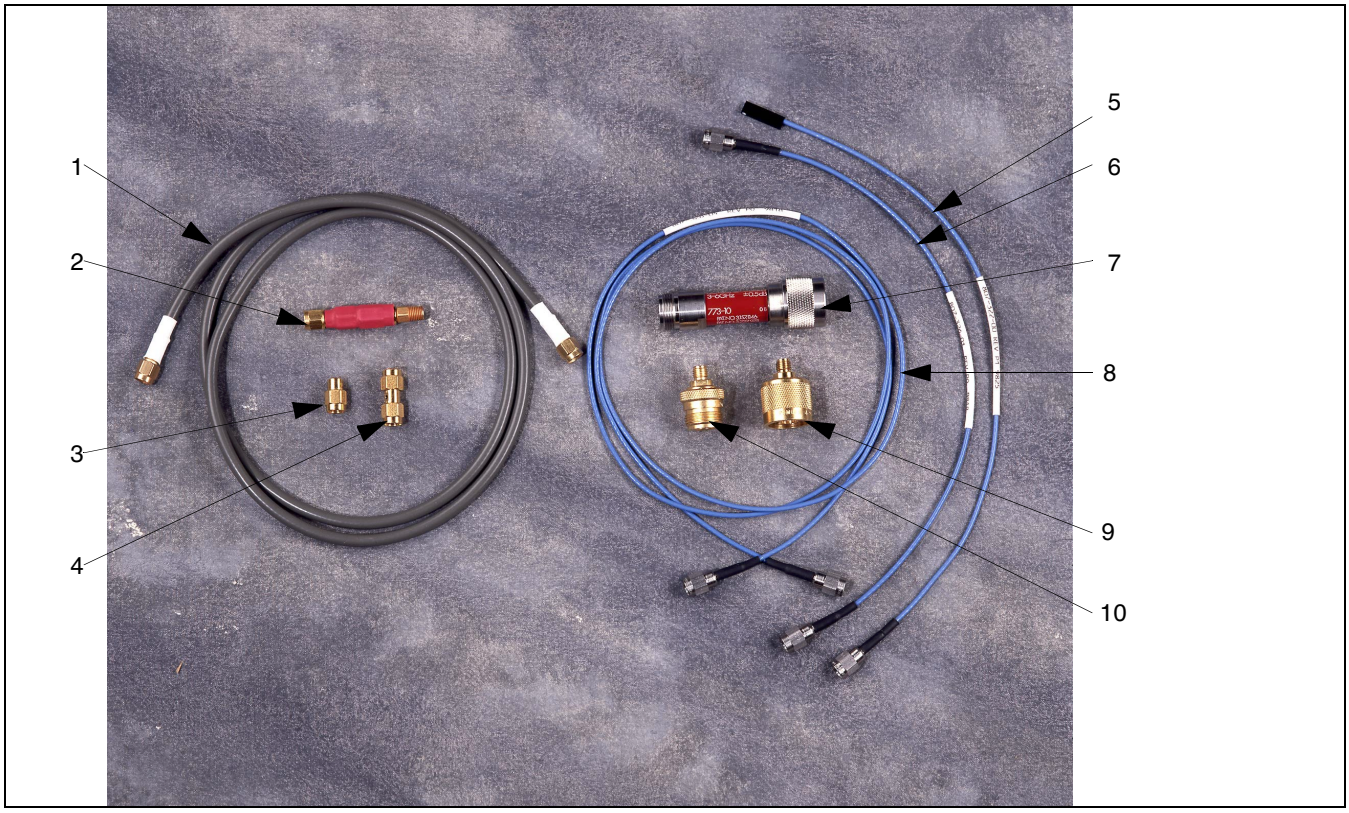
Digital instrument interfacing is accomplished on a channel-by-channel basis with each of the 384 possible digital channel outputs being identified. Each channel has an accompanying ground signal. (For more information on ground signals, see Ground Signals.)

The figure LA785 Digital Channel Interface Pins provides a magnified view of one area of the digital interface. Due to spacing constraints on the DIB, the full channel numbers could not be silk-screened onto the DIB adjacent to the connector. Therefore, for each group of eight signals represented by a test head channel card, the first and last signals are full labeled. For the remaining six signals, only the last digit of the channel number is silk-screened. Interfacing to each of the digital signals is performed by connecting a cable (pn 807-322-00) to the appropriate pair of header pins. Note that the coaxial cable (pn 807-322-00) provides a white dot on the 2-pin header housing. This dot indicates the location of the outer conductor of the cable. The outer conductor (or shield) must always be connected to a DIB ground signal. The LA785 DIB silk-screen information provides the slot number and pin location of the signal (center conductor).



LA785 Digital Channel Interface Pins

Catalyst Level IV Kit (pn 803-806-00) Information



LA785 Interface Cables

Interface Cables

Item	Part Number	Description
1	918-242-00	3ft SMA (M)/SMA (M) Scope Cable
2	804-878-00	HSD Scope Probe Assembly
3	359-083-01	50 Ohm SMA Terminator
4	359-256-00	SMA M/M Adapter
5	807-322-00	1ft SMA (M)/2 Pin Header Cable
6	807-326-01	1ft SMA (M/M) Cable (Part of 803-804-00 Kit)
7	733-108-00	10 dB Attenuator (N)
8	807-326-04	4ft SMA (M/M) Cable
9	359-164-00	SMA (F)/N (M) Adapter
10	359-147-00	SMA (F)/N (F)
Not Shown	358-216-15	15ft BNCC (M/M) Cable
Not Shown	465-527-00	Torque Tool (8 in-lb.)
Not Shown	465-528-00	Wrench Head (5/16 in)

Definitions

Calibration

Calibration

Comparison of a measurement standard or instrument of known accuracy with another standard or instrument to detect, correlate, report, or eliminate by adjustment, any variation in the accuracy of the item being compared.

Autocalibration

The calibration of a system or subset of a system that does not require operator interaction to run.

External Calibration

Calibration of a test system instrument or test system standard with a check standard or transfer standard.

Adjustment

The changing of circuit inputs or circuit components to achieve a desired performance. Adjustments may be permanent or periodic and may be manual or automatic.

Deskew

The alignment of edges for a high-speed digital channel.

Checkers

ST Checker

A self test (ST) program that achieves the test objectives without use of any external fixtures or instrumentation. The objective of this program is that it can be run without disturbing the device setup.

MI Checker

A maintenance and installation (MI) program that requires some type of external fixtures or instrumentation. This type of program typically is used to check the final connection path out to the device location. We recommend it be run only during initial system installation and during each preventative maintenance session.

Other

ESSD (Engineering Specification Support Document)

Official controlled document listing all specifications for a particular instrument or subsystem, which outlines how and when the performance against specification is verified.

Tolerance (out of)

Beyond the allowable deviation from the expected value.

Performance Verification

The process where a test system's performance against specifications is verified. There are different categories of performance verification such as tolerance verification, functional verification, and design verification.

Traceability

The definition of traceability used by Teradyne is derived from Dr. Brian Belanger's (NIST) definitions of traceability.

- Traceability means the ability to relate individual measurement results to national standards or nationally accepted measurement systems through an unbroken chain of comparisons.

Primary Standard (Reference)

Reference systems are of the highest accuracy order in a calibration system (that is, standard cells, 4 terminal-oil bath resistors, and so on). They are the basis for defining Teradyne's accuracy, and are regularly compared against national standards.

Transfer Standard

Designated measuring equipment used in a calibration system as a medium for transferring the basic value of reference standards to lower-echelon transfer standards or measuring equipment.

Check Standard

A stable, characterized in-house standard that is calibrated at periodic intervals to ensure that it is in tolerance (documented control).

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358-216-04 34, 69
358-216-15 81, 82, 138
358-692-00 34

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359-083-00 75
359-083-01 138
359-147-00 138
359-149-00 75
359-164-00 81, 82, 138
359-256-00 138

465 Part Numbers
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733 Part Numbers
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800 Part Numbers
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800-487-00 59, 65
800-537-02 48

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